F 3322 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2014

Seventh Semester

Branch : Electronics and Communication Engineering

EC 010 701—VLSI DESIGN (EC)

(New Scheme—2010 Admission onwards—Regular/Supplementary)

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 3 *marks.*

1. Discuss the used for annealing after non implantation.
2. Write a note on IC cross overs.
3. Write a note on latchup in CMOS.
4. Discuss the need for scaling of transistors.
5. Figure out the salient features of GaAs technology.

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. Write a note on wire bonding.
7. Explain junction isolation.
8. Explain the VI characteristics of a CMOS inverter.
9. Explain a CMOS transmission gate. What are its features ?
10. Explain the crystal structure of GaAs.

(5 × 5 = 25 marks)

Part C

Answer **all** *questions.*
Each question carries 12 *marks.*

11. Explain FZ process for obtaining single crystalline Si. Compare FZ grow Si with a Cz grown Si.

Or

12. Explain how EGS can be obtained from its raw materials.

Turn over

13. Explain the different steps involved in IC fabrication to control the VT of MOS transistors.

Or

14. Explain monolithic diode and transistors. How are they fabricated ?

15. Discuss the CPL realisation of a two input NAND gate. Compare it with a CMOS NAND gate.

Or

16. Explain the TG realisation of an XOR gate. How is it different from a CMOS logic ? Compare them.

17. Explain the Bi CMOS structure of a NAND gate. Compare it with a CMOS NAND structure.

Or

18. Explain different approaches to scaling. How does these affect the electrical and physical parameters of a MOSFET ?

19. (a) Explain the different steps in MESFET fabrication. (8 marks)

(b) Write a note on FPGASS. (4 marks)

Or

20. Explain the doping process and channeling effect in GaAs technology.

[5 × 12 = 60 marks]