G 1553 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2015

Fourth Semester

Branch : Electrical and Electronics Engineering

EE 010 405—DIGITAL SYSTEMS AND COMPUTER ORGANISATION (EE)

(New Scheme—2010 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 3 *marks.*

1. Define the terms : Fan In and Fan Out.
2. What are Asynchronous Inputs ?
3. What is a shift Register ?
4. What are serial Adders ?
5. Explain Cache hit and Cache miss.

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. Compare combinational and sequential circuits.
7. Discuss the disadvantages of Ripple counters.
8. Explain the operation of a Ring Counter.
9. Write the advantages of Parallel Adders.
10. Explain Virtual memory.

(5 × 5 = 25 marks)

Part C

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. Explain with a figure, the operation of a TTL NAND circuit.

Or

Turn over

12. Minimise the 4 variable logic function using Kmap.

$f(A, B, C, D) = \Sigma_m (0, 1, 2, 3, 5, 7, 8, 9, 11, 14)$

Realise the function using NAND gate.

13. Explain a Mod 10 ripple counter with a neat figure.

Or

14. (a) What is Race around condition ? (3 marks)

(b) Explain with a figure, using gates, how JK flipflop can be converted to T flip flop. (9 marks)

15. Explain Universal shift Register with a neat figure.

Or

16. Design a mod 12 synchronous counter.

17. (a) Discuss the steps to design a logic unit. (6 marks)

(b) Explain 1 stage ALU. (6 marks)

Or

18. (a) Draw the block diagram of a Processor and explain in detail. (6 marks)

(b) Explain the processor Bus structures. (6 marks)

19. (a) Discuss the principles and Organization of static and Dynamic RAM cells. (7 marks)

(b) Explain the principle of memory Interleasing. (5 marks)

Or

20. (a) Explain USB with a block diagram.

(b) Explain SCSI.

[5 × 12 = 60 marks]