G 530 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2014

Fourth Semester

Branch : Electrical and Electronics Engineering

EE 010 405—DIGITAL SYSTEMS AND COMPUTER ORGANIZATION (EE)

(New Scheme—2010 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 3 *marks.*

1. State DeMorgan's theorem.
2. What is the difference between latch and flip-flop ? Explain.
3. Differentiate synchronous counter from asynchronous counter.
4. What is the principle of Fast Adder ? Explain.
5. Explain the principle of memory interleaving. Explain.

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. Define and explain the parameters of logic families.
7. Explain the truth tables and excitation tables of JKFF and SRFF.
8. Draw a ring counter and explain it in detail.
9. Draw the block diagram of a processor and explain it in detail.
10. Differentiate ROM from RAM .Explain the difference.

(5 × 5 = 25 marks)

Part C

Answer **all** *questions.*
Each question carries 12 *marks.*

11. (i) Explain a 4 : 1 MUX with a neat schematic diagram.

    (ii) Draw a BCD to decimal decoder and explain it.

Or

Turn over

12. (i) Draw CMOS NAND and NOR gates . Explain them in detail.

(ii) Differentiate CMOS and TTL logic families.

13. Realize a JKFF from SRFF using only NAND gates. Explain the procedure in detail.

Or

14. Draw an asynchronous UP- DOWN counter and explain its design procedure in detail.

15. Explain the types of shift registers in detail with neat diagrams.

Or

16. (i) Design a 2 bit up down synchronous counter and realize the same using JKFF.

(ii) Differentiate counters from shift registers.

17. Explain a full adder circuit with a neat block diagram. Design a full adder using the basic gates.

Or

18. (i) Explain the steps to design one stage of ALU with a neat diagram.

(ii) Explain the processor bus structure in detail, with a neat diagram.

19. Explain the Static and Dynamic RAM cells with diagrams. Explain the features of flash memory and cache memory.

Or

20. (i) Draw the block diagram of USB and explain it in detail.

(ii) Give an account on :

(a) EPROM ;

(b) Virtual memory ;

(c) Hit and Miss.

(5 × 12 = 60 marks)