G 1575 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2015

Fourth Semester

Branch : Electronics and Communication/ Applied Electronics and Instrumentation/ Electronics and Instrumentation Engineering

DIGITAL ELECTRONICS AND LOGIC DESIGN (LAS)

(Old Scheme—Prior to 2010 Admissions)

[Supplementary/Mercy Chance]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 4 *marks.*

1. Realise the logic expression $F = XY + YZ + \overline{X}\,Y\overline{Z}$ using NAND gates.
2. What are logic families ? Compare TTL and CMOS logic families.
3. What is a demultiplexer ? Explain with an example circuit.
4. Plot the K-map for $\overline{A}BC + A\overline{B}C + AB\overline{C} + ABC$.
5. Draw the full adder using half adders.
6. Subtract using (i) 2's complement method and (ii) 1's complement method : 1010101–110011.
7. Draw the D-flip-flop with the logic diagram and truth table and explain.
8. Convert an SR flip-flop into (i) D and ; (ii) T flip-flops.
9. Distinguish between RAM, ROM and PROM. Which is volatile ?
10. Draw the circuit diagram, output sequence and timing diagram of a 3 bit ring counter ?

(10 × 4 = 40 marks)

Part B

Answer **all** *questions.*
Each question carries 12 *marks.*

11. Explain the circuit diagram and working of a three-input TTL NAND gate. Why totempole output stage is used ? Sketch and explain its voltage transfer characteristics.

Or

12. What are universal logic gates ? Why they are called so ? Using them, show how (i) NOT ; (ii) AND ; (iii) OR ; (iv) EX-OR logics can be realised ?

Turn over

13. Using k-maps, obtain the SOP and POS forms for $Y = \bar{A}BC + \bar{A}\bar{B}C + ABC$. Implement using (i) only NOR gates ; (ii) Basic logic gates.

Or

14. Implement the following functions using decoder minimizing the number of inputs to be summed (a) $f_1 = \Sigma(0, 2, 3, 5, 6, 7)$; (b) $f_2 = \Sigma(1, 3, 4, 6, 7)$.

15. With a circuit diagram, explain the working of a 4 bit parallel binary adder.

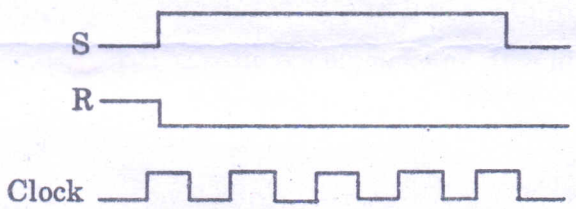
Or

16. With a neat circuit diagram explain the working of a 4 bit serial subtractor.

17. What is the race around condition ? How it is eliminated in master-slave circuit ? Draw a clocked MS JK flip-flop with asychronous inputs and explain.

Or

18. The figure below shows the input waveforms applied to S, R and clock terminals of an SR flip-flop. Draw the waveforms of Q and $\overline{Q}$. Explain the output states ?



19. Design a mod 12 binary counter using excitation table and K-maps. Draw its circuit and timing diagrams.

Or

20. Describe the internal structure of a ROM having square register array and capable of storing 1K bytes.

(5 × 12 = 60 marks)