F 3087

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B.TECH. DEGREE EXAMINATION, NOVEMBER 2014

Third Semester

Branch : Computer Science and Engineering

MICROPROCESSOR SYSTEMS (R)

(Prior to 2010 Admissions—Old Scheme)

[Supplementary/Mercy Chance]

Time : Three Hours

Maximum : 100 Marks

Part A

*Answer **all** questions briefly.*
Each question carries 4 marks.

1. Give the flag register format of 8085 and explain each flag.

2. Explain with schematics, how separate address, data signals can be generated from 8085 common address/data lines.

3. Write and explain two methods to initialise stack pointer and FFFFH.

4. Is it possible to check the AC flag status of 8085 ? Explain.

5. Explain the various steps involved while executing CALL instruction with an example.

6. What is subroutine ? How is it useful ? Explain.

7. Distinguish between hardware and software interrupts.

8. Explain how 8085 responds to INTR interrupt.

9. List the important points which must be considered while interfacing memory devices in 8085.

10. Write a short note on serial communication supported by 8085.

(10 × 4 = 40 marks)

Part B

*Answer **all** questions.*
Each full question carries 12 marks.

11. What is the maximum memory that 8085 can address ? Write neat block schematics, describe how the memory is organised and the chip select signals designed ?

Or

12. Describe the various address, data and control pins of 8085.

Turn over

13. Explain the operations of the following instructions and specify their addressing modes and show the machine cycles :—

    (i)   DAA ;   (ii)   XTHL ;

    (iii) ADCr ;   (iv) CMP M.

Or

14. Explain the operations performed by 8085 when the following instructions are expected :—

    (i)   SPHL ;   (ii)   RAR ;

    (iii) DADrp ;   (iv) XRA r.

Also show how the flags are affected in each case ?

15. Explain BCD to binary code conversion technique and write an ALP for the same.

Or

16. Draw and explain the :—

    (i)   Memory write and ;

    (ii)   I/O read cycle of 8085.

17. With the help of a neat flow chart, describe the polling routine in 8085.

Or

18. Draw the block diagram of 8259 and explain the function of each block.

19. An 8 KB ROM having a word length of 8 bits is to occupy the first 8 kB of the address space of an 8085. Two 2KB RAMs having word lengths of 4 bits each are to occupy 2KB starting from address 4000 H. Draw and design address decoding logic.

Or

20. With a block schematic of a DMA controller, explain the functions of each signal connected to it. Explain how the DMA controller effects the data transfer between memory and peripheral devices.

$(5 \times 12 = 60$ marks)