Course code	Course name	L-T-P-Credits	Year of introduction
AE363	VLSI CIRCUIT DESIGN	3-0-0-3	2016

Prerequisite : Nil

Course Objective

- To bring circuits and system views on design together.
- To understand the design of digital VLSI circuits for hardware design.

Syllabus

Fundamental considerations in IC processing - NMOS IC technology - CMOS IC technology - BiCMOS IC technology- The MOS device- capacitance of MOS structure – characteristics- Second order MOS device effects- pass transistors and transmission gates -The basic inverter using NMOS- Basic NAND, NOR circuits - The CMOS inverter, - pseudo CMOS- Layout design of static MOS circuits –Stick Diagram –Fabrication-- Combinational circuits- Timing issues in VLSI system design.

Expected outcome

The students will be able

i. to learn layout, stick diagrams, fabrication steps , static and switching characteristics of inverters
ii. to design digital system using MOS circuits.

Text Books

1. Douglas A. Pucknell & Kamran Eshraghian, *Basic VLSI Design*, PHI.
2. Jan M. Rabaey, A. Chandrakasan, B. Nikolic, *Digital Integrated Circuits- A Design perspective*, 2/e, Pearson education.
3. Sung-Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits Analysis and Design, Tata Mc-Graw-Hill

References

1. Charles H Roth Jr – *Fundamentals of Logic Design* 4 Ed, Jaico Publishers
2. Mead & Conway , *Introduction to VLSI System Design*-Addison Wesley
3. S M Sze, VLSI Technology, PHI
4. Wayne Wolf: *Modern VLSI Design Systems on Chip*-Pearson Education, 2nd ed.,
5. Weste and Eshraghian, *Principles of CMOS VLSI Design*, A Systems Perspective,2/e, Pearson Education.

Course Plan

Module	Contents	Hours	Semester exam marks
I	VLSI process integration: - fundamental considerations in IC processing - NMOS IC technology - CMOS IC technology - BiCMOS IC technology - GaAs technology. Ion implantation in IC fabrication.	6	15%
II	The MOS device: (n - channel & p- channel) - capacitance of MOS structure - accumulation, depletion and inversion, threshold voltage, current equations - characteristics, channel pinch-off. Second order MOS device effects: short-channel effect, narrow width effect, sub-threshold current, device saturation characteristics.	6	15%
FIRST INTERNAL EXAMINATION			
III	Switch logic- pass transistors and transmission gates, Gate logic-The basic inverter using NMOS-circuit – current	8	20%

	equations - pull up to pull down ratio- transfer characteristics- Alternate forms of pull up. Basic NAND, NOR circuits. The CMOS inverter, characteristics – NAND, NOR and compound circuits using CMOS. Other forms of CMOS logic: pseudo CMOS, CMOS domino logic, n-p logic.		
IV	Layout design of static MOS circuits – Layout rules - general principles & steps of lay-out design - use of stick diagrams - design rules - Layout examples of NAND and NOR-Fabrication.	7	15%
SECOND INTERNAL EXAMINATION			
V	Combinational circuits - clocked sequential circuit - drivers for bus lines. Scaling of MOS circuits: scaling models and scaling factors for device parameters.	7	15%
VI	Timing issues in VLSI system design: timing classification- synchronous timing basics – skew and jitter-latch based clocking- self timed circuit design - self timed logic, completion signal generation, self-timed signalling– synchronizers and arbiters	8	20%
END SEMESTER EXAMINATION			

QUESTION PAPER PATTERN:

Maximum Marks:100 Exam Duration: 3 Hours

Part A

Answer any two out of three questions uniformly covering Modules 1 and 2 together. Each question carries 15 marks and may have not more than four sub divisions.

(15 x 2 = 30 marks)

Part B

Answer any two out of three questions uniformly covering Modules 3 and 4 together. Each question carries 15 marks and may have not more than four sub divisions.

(15 x 2 = 30 marks)

Part C

Answer any two out of three questions uniformly covering Modules 5 and 6 together. Each question carries 15 marks and may have not more than four sub divisions.

(20 x 2 = 40 marks)