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SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

SIXTH SEMESTER B.TECH DEGREE EXAMINATION(R,S), MAY 2024

B. Tech. Electronics and Communication Engineering

(2020 SCHEME)

Course Code : 20ECT304

Course Name : VLSI Circuit Design

Max. Marks : 100 **Duration:3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Differentiate ASIC and FPGA.
2. Define static and dynamic power consumption in ASIC.
3. Implement a NAND gate using transmission gate.
4. Define V_{IL} and V_{IH} for a CMOS inverter.
5. What are the advantages of NORA Logic?
6. How does a sensing amplifier contribute to the operation of an SRAM?
7. Explain the term 'critical path' in the context of adder design.
8. Describe the purpose of carry-skip adders, and how do they mitigate carry propagation delay.
9. Describe the applications of metal layers deposited in VLSI devices.
10. What is meant by wafer inspection in VLSI fabrication?

PART B

(Answer one full question from each module, each question carries 14 marks)

MODULE I

11. a) What is Logical design? Explain its relevance in ASIC design. 7
    b) Explain the Top-Down Design methodology with the help of a diagram. 7

OR

12. a) Explain the advantages of Systen on Chip(SoC). 7
    b) What are the advantages of Semi-Custom ASIC over Full Custom ASIC design? 7

MODULE II

13. Illustrate the operation of 2:1 and 4:1 multiplexer using transmission gates. 14

OR

14 Explain the factors influencing the rise and fall time of CMOS logic signals. How do parameters such as load capacitance, transistor sizes, and parasitic capacitances affect signal transition times in CMOS circuits? Describe the strategies for minimizing rise and fall times to improve circuit performance. 14

MODULE III

15. Explain the architecture and operation of Static Random Access Memory (SRAM). Compare and contrast SRAM with Dynamic RAM (DRAM) in terms of structure, performance, and power consumption. 14

OR

16. Explain the principle and operation of dynamic logic circuits in digital circuit design. Explore the advantages and limitations of dynamic logic compared to static CMOS logic, and analyze the key factors influencing their performance. 14

MODULE IV

17. With the block diagram illustrates the principle of operation of a linear carry select adder. 14

OR

18. a) Explain the working of 3x3 array multiplier. 7
    b) Estimate the delay of an n bit carry skip adder. 7

MODULE V

19. Describe the principles and operation of Molecular Beam Epitaxy (MBE) in the context of semiconductor materials growth. How does MBE enable precise control over thin film deposition at the atomic level, and what are the key factors influencing epitaxial growth in this technique? 14

OR

20. Explore the principles, techniques, and applications of etching in VLSI fabrication. Explain the various etching methods, including wet etching, dry etching (plasma etching), and chemical mechanical planarization (CMP). 14

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