Register No: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

SECOND SEMESTER INTEGRATED MCA DEGREE EXAMINATION (R,S), MAY 2024
(2020 SCHEME)

Course Code: **20IMCAT106**

Course Name: **Introduction to Digital Systems & Logic Designs**

Max. Marks: **60** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Convert $(110101)_2$ and $(111001)_2$ to decimal.
2. Convert $(100011110101)_2$ to hexa decimal number.
3. Implement AND gate using NOR gate.
4. Prove A(A+B)=A.
5. Write a short note on MS flip flop.
6. Convert ABD+ACD+BCD to standard SOP.
7. Draw the circuit diagram of 2 to 4 decoder.
8. Explain 2 bit comparator with an example.
9. Explain serial-in serial-out shift register.
10. What is SOC system model?

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

11. Represent -45 in 8-bit sign magnitude, 1's complement and 2's complement form. (6)

OR

12. Do the following operations. (6)
    i. 10110 + 1001
    ii. 1110 - 111
    iii. 10110 * 101

MODULE II

13. Describe the basic gates in detail. (6)

OR

14. Explain the laws and rules of boolean algebra. (6)

MODULE III

15. Minimize the boolean expression $f(A,B,C,D)=\Sigma\{0,2,3,4,5,6,8,10,11,12,13,14\}$. (6)

OR

16. Compare T flip flop and D flip flop. (6)

MODULE IV

17. Design a half adder. (6)

OR

18. With a diagram, explain 8x1 multiplexer. (6)

MODULE V

19. Discuss the working of Parallel-In Serial-Out shift register. (6)

OR

20. Design a 3 bit synchronous counter. (6)

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