Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

THIRD SEMESTER B.TECH DEGREE EXAMINATION (R,S), DECEMBER 2023
ELECTRONICS AND COMMUNICATION ENGINEERING
(2020 SCHEME)

Course Code: **20ECT203**

Course Name: **Logic Circuit Design**

Max. Marks: **100** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Convert the following numbers from the given base to the bases indicated
   (a) $(250.55)_{10}$ to hexadecimal
   (b) $(357)_8$ to decimal
2. Subtract $(1111)_2$ from $(11000)_2$ using 1's complement and 2's complement method.
3. Express the following Boolean function in canonical form of POS
   $$F(x, y, z) = x'+yz+xz'+xy'z'+xyz'$$
4. State and prove De-Morgan's Theorems.
5. A function is defined as F(a,b,c,d) = a'b+a'c+c'+a'd+a'b'c'+a'bc. Implement the function using single 8:1 MUX.
6. Implement a half subtractor circuit using NAND gates only.
7. Differentiate between a latch and a gated latch.
8. Write the excitation tables and characteristic equation of D and T flip-flops
9. Define fan-in and fan-out of logic gates.
10. Define Propagation delay of logic families.

PART B

(Answer one full question from each module, each question carries 14 marks)

MODULE I

11. a) Determine the Hamming code for the information 1011, with even parity. (5)
    b) Explain the format of single precision floating point representation and find the decimal value corresponding to the given floating point number. (11000001011110110000000000000000) (5)
    c) Perform the following decimal operations in the 8421 BCD code
    a) (372) + (388) b) (716) − (598) (4)

OR

12. a) Represent 101011 in BCD, Excess 3 and Grey code (6)

b) Perform the following operations: (4)

i. $(E39)_{16} + (3F9)_{16}$

ii. $(721)_8 - (32)_8$

c) What is alphanumeric codes? How it is useful in digital computers? (4)

MODULE II

13. a) Simplify using K-map and implement the real minimal expression using NOR gates (9)

$f = \pi M\ (4,6,7,8,10,11,12,15).d(3,5)$

b) Expand A+BC'+ABD'+ABCD to minterms and maxterms (5)

OR

14. a) Reduce the following expressions using K-map and find the real minimal expression. (7)

$F\ (W,X,Y,Z) = \sum (0,1,2,3,5,7,8,9)+d(10,12,13)$

b) Write a Verilog code to implement the given function using NAND gates only. (7)

A'BC' + AB'C

MODULE III

15. a) Realize a 3 bit comparator. (7)

b) Implement a 8:1 MUX using 2:1 MUX only. (7)

OR

16. a) Explain the working of four bit Ripple Carry Adder. (7)

b) Design and implement a full subtractor using two half subtractors. (7)

MODULE IV

17. a) Realize the following: (8)

i) T flip-flop using SR flip-flop ii) JK flip-flop using D flip-flop

b) With the logic diagram explain the working of a four bit bi-directional Serial in Serial out (SISO) shift register with mode control. (6)

OR

18. a) Design a MOD-7 synchronous counter using JK flip-flop. When the counter enters an unused state, the counter has to start counting from 0. Draw the timing diagram. (9)

    b) What is race around condition? How it is avoided? (5)

MODULE V

19. a) Compare TTL, ECL and CMOS logic families in terms of their characteristics. (6)

    b) Draw the circuit and explain the operation of TTL NAND gate. (8)

OR

20. a) Draw and explain the circuit diagram of a standard 2 input CMOS NOR gate. (7)

    b) Explain in detail about totem pole TTL NAND gate with the help of a diagram. (7)

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