Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

THIRD SEMESTER B. TECH DEGREE EXAMINATION (R,S), DECEMBER 2023
ROBOTICS AND AUTOMATION
(2020 SCHEME)

Course Code : **20RBT205**

Course Name: **Digital Electronics**

Max. Marks : **100** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Convert the decimal number 215 to following codes
   (i)BCD code (ii)Excess 3 code (iii) Gray code
2. Define the terms: (i) Noise Margin (ii) Fan-out
3. Express $f(A, B, C) = AB + A\bar{C} + BC$ in standard SOP form.
4. List the limitations of Karnaugh map.
5. Explain race around condition.
6. Design and draw the circuit of an asynchronous Mod-12 counter.
7. With a neat figure, derive the output, V_{out} of a Weighted Resistor type DAC.
8. An 8-bit Successive Approximation ADC has a resolution of 30 mV. What will its digital output be for an analog input of 2.86 V?
9. Differentiate between PLA and PAL.
10. Define **reg** and **net** in Verilog HDL.

PART B

(Answer one full question from each module, each question carries 14 marks)

MODULE I

11. a) Write Notes on (i) ASCII Code (ii) Excess-3 code (iii) Gray Code (9)
    b) Compare TTL and CMOS logic families in terms of fan-in, fan-out, supply voltage, propagation delay and noise margin. (5)

OR

12. a) Covert each decimal number to binary and perform the subtraction 21.5_{10} -13.25_{10} using (i)1's complement method & (ii) 2's complement method. (6)
    b) Describe the working of a 2-bit TTL NAND gate with Totem pole configuration. (8)

MODULE II

13. a) Implement the following functions using 4:1 MUX (8)

(i) 2 input AND
(ii) 2 input XOR
(iii) f (A, B, C) = Σ_m (0, 3, 5, 6)

b) Design an 8:3 encoder. (6)

OR

14. a) Design a full subtractor circuit using NAND gates only. (8)
b) Implement a full adder using a 3:8 decoder. (6)

MODULE III

15. a) With the help of necessary steps, convert an S-R flip-flop to J-K flip-flop. (8)
b) Explain the asynchronous inputs of a flip-flop. (6)

OR

16. a) With a neat figure, explain the advantages and working of a Master-Slave J-K flip-flop. (9)
b) Derive the characteristic equation of a S-R flip-flop. (5)

MODULE IV

17. a) With neat illustrations, explain an R-2R ladder type DAC and calculate V_{out} when input is (i) 1000 and (ii) 0100. (8)
b) Design a 4-bit weighted resistor DAC whose full-scale output voltage is -5V. The logic levels are 1=+5V and 0=0V. What is the output voltage when the input is 1101? (6)

OR

18. a) With the help of a block diagram, explain Flash type ADC. (6)
b) Explain the parameters of Analog to Digital Converter. Determine the full-scale output voltage and percentage resolution of a 6-bit DAC for a step size of 50mV. (8)

MODULE V

19. a) Explain the different level of abstractions in Verilog HDL. Give an example for each level of modelling. (8)
b) Write a program for a 4-bit Ripple Carry Adder using gate level modelling in Verilog. (6)

OR

20. a) Explain, Keywords, Identifiers and Operators in Verilog HDL. (10)
b) Write a program for a 4:1 Multiplexer in Verilog using Gate level modelling. (4)

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