Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

THIRD SEMESTER INTEGRATED MCA DEGREE EXAMINATION (R), DECEMBER 2023
(2020 SCHEME)

Course Code: **20IMCAT201**

Course Name: **Computer Organization**

Max. Marks: **60** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Mention the two registers used for communicating to memory and define each.
2. List the differences between program controlled I/O and memory mapped I/O.
3. What are the steps involved in the execution of an instruction? Explain with an example.
4. What do you understand by microinstruction and micro routine?
5. With the help of a diagram or truth table demonstrate the addition of signed numbers.
6. Explain 4 bit carry look ahead adder with necessary diagram.
7. Write short note on DMA.
8. What do you mean by pipelining? Why do we need pipelining?
9. Mention differences between asynchronous DRAM and synchronous DRAM.
10. What is the significance of cache memory?

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

11. Explain single bus architecture. (6)

OR

12. a) List all addressing modes. (2)
    b) Elaborate any four addressing modes by citing examples. (4)

MODULE II

13. Comment on multiple bus organization with necessary diagrams. (6)

OR

14. Explain how processor use hardwired control to generate control signals. (6)

MODULE III

15. With the help of diagrams explain how addition and subtraction logic is realized in system. (6)

OR

16. Illustrate Booth algorithm. (6)

MODULE IV

17. Explain the working of the interrupt mechanism. (6)

OR

18. Explain the concept of instruction pipelining and its impact on the throughput of a processor. (6)

MODULE V

19. Write short note on different types of read-only memories. (6)

OR

20. Explain (6)
    i) Direct Mapping
    ii) Associative Mapping
    iii) Set-Associative Mapping

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