

Register No.: Name:

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

THIRD SEMESTER B.TECH DEGREE EXAMINATION (S), FEBRUARY 2023 ELECTRONICS AND COMMUNICATION ENGINEERING

(2020 SCHEME)

Course Code: 20ECT203

Course Name: Logic Circuit Design

Max. Marks: 100

Duration: 3 Hours

PART A

(Answer all questions. Each question carries 3 marks)

1. Differentiate weighted and non-weighted codes with examples.
2. Explain data types in Verilog.
3. What are minterms and maxterms?
4. A staircase light is controlled by two switches, one at top and another at bottom. Make a truth table for this system.
5. Draw the circuit diagram of a single bit comparator.
6. Write the truth table and derive the expression for a half subtractor.
7. Distinguish between synchronous and asynchronous inputs of flip flops.
8. Draw the circuit diagram of a 3-bit Johnson counter.
9. Define the terms fan-in and fan-out of a logic gate.
10. Differentiate between open collector and totempole configurations of TTL.

PART B

(Answer one full question from each module, each question carries 14marks)

MODULE I

11. a) Explain binary to gray and gray to binary conversion with examples. (8)
b) Explain the principle behind parity checking. Attach an odd parity bit for the following data. (6)
i. 11010010 ii. 10010001

OR

12. a) List the advantages of 2's complement over 1's complement. (8)
Perform 2's complement subtraction of
i. 11001010 - 1110011 ii. 10111001 - 11011101.
b) Convert each of the following to decimal (6)
i. $(11011.101)_2$ ii. $(537.25)_8$ iii. $(BC1.0E)_{16}$.

MODULE II

13. a) Minimize the function $f = \sum m(0,2,6,9,10,14,15)$ using a K-map and realize it using NAND gates. (10)
- b) Rewrite in standard POS form $(AB)+(C)$. Also write the truth table. (4)

OR

14. a) Simplify using K-map, $f = \pi(2,3,4,9,12,14)$. Implement the expression using NOR gates. (10)
- b) Prove that bubbled NAND gate is equivalent to OR gate (4)

MODULE III

15. a) Draw the circuit diagram and explain the operation of a BCD adder with an example. (8)
- b) Draw logic circuit that receives 4 inputs and selects one among them as output. Write Verilog code for the same. (6)

OR

16. a) Realise a full adder using 3:8 decoder. (8)
- b) Write Verilog code for half adder using NAND gates. (6)

MODULE IV

17. a) Design a mod 6 synchronous counter using JK flipflops. (10)
- b) Write Verilog code for T flipflop. (4)

OR

18. a) Draw the circuit diagram of a four-bit asynchronous upcounter. Explain its operation using timing diagram. (8)
- b) Write Verilog code for 3-bit down counter. (6)

MODULE V

19. a) Explain the operation of CMOS NAND and NOR gates with necessary diagrams. (8)
- b) Explain noise margin of TTL. (6)

OR

20. a) Draw the circuit diagram of a TTL NAND gate and explain its operation. (8)
- b) Compare TTL and CMOS gates in terms of speed, power consumption and noise margin (6)
