Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

THIRD SEMESTER B.TECH DEGREE EXAMINATION (S), FEBRUARY 2023
ROBOTICS AND AUTOMATION
(2020 SCHEME)

Course Code : 20RBT205

Course Name: Digital Electronics

Max. Marks : 100 **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Convert the following Decimal numbers to Binary
   a) 127 b) 508
2. Draw the circuit diagram of the CMOS NAND gate.
3. State and prove De Morgan's First and Second theorems.
4. Draw the logic diagram of a 2:1 multiplexer
5. Draw the block diagram diagram of T Flip Flop and show its input output relationship.
6. Draw the timing diagram of a 2-bit asynchronous up counter
7. Write a short note on the significance of Digital to Analog Converter in Robotic design
8. Define the Accuracy and Precision of Analog to Digital converters.
9. What is Dynamic RAM? Draw the circuit of One Transistor Dynamic RAM Cell.
10. Write the Verilog HDL code for a Half Adder.

PART B

(Answer one full question from each module, each question carries 14 marks)

MODULE I

11. a) Perform each of the following subtractions of the signed numbers using 2's complement method (6)
    (i) 00110010 – 00001111 (ii) 01100100 - 11100111
    b) Draw the standard logic symbols and generate the truth table for any 4 logic gates (8)

OR

12. a) With the help of examples, explain Gray to Binary and Binary to Gray code conversions. (7)
    b) Draw the circuit of the CMOS NOR gate and explain its operation and characteristics. (7)

MODULE II

13. a) Simplify the following Boolean expression and realize the circuit. (5)
F (A, B, C, D) = A'C+A'BC'D'+A'B'C
b) Simplify the following Boolean functions using the Karnaugh map and realize the logic circuit using basic logic gates. (9)
F (W, X, Y, Z) = Σ m (0,1,2,4,5,10,12,13,14) + Σ d (6,8,11).

OR

14. a) Draw and explain a 4-bit parallel adder. (8)
b) What is a Demultiplexer? Draw and explain the operation of a 1:4 demultiplexer. (6)

MODULE III

15. a) With the help of a logic diagram explain S R Flip Flop. (7)
b) What is the need for a Master-Slave connection of JK Flip Flop? Use the functional diagram to explain the operation. (7)

OR

16. a) Describe the functions of Serial In Serial Out (4-bit) shift register with the help of a diagram. (6)
b) Design an asynchronous MOD-8 up counter and explain its operation with the help of a timing diagram. (8)

MODULE IV

17. a) Illustrate the working of the R-2R ladder DAC. (7)
b) What are the specifications of DAC 0808? Write a short note on its functions. (7)

OR

18. a) Illustrate the working principle of successive approximation ADC. (7)
b) Draw the basic diagram of ADC0808 and write down its features. (7)

MODULE V

19. a) Draw the circuit of a 6T SRAM and explain its operation. (8)
b) Realize the following function using PLA. (6)
F1= ∑(2,3,6,7) , F2 = ∑(0,1,4,7)

OR

20. a) What are the main components of an FPGA? Draw the basic block diagram and explain its functions. (8)
b) Write down the Verilog HDL code for a D Flip Flop. (6)

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