G 1244 (Pages : 3) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2015

Sixth Semester

Branch : Applied Electronics and Instrumentation

A1 010 606 L 03—DIGITAL SYSTEM DESIGN (Elective I) (AI)

(New Scheme—2010 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 3 *marks.*

1. What is the basic architecture of PLA ?
2. What are the characteristics of RS 232 ?
3. Compare mealy and more machines.
4. Which are the different data types used in VHDL ?
5. What are the different attributes used in VHDL ?

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. Explain PROM architecture in detail.
7. Explain the characteristics of PCI bus.
8. Draw the state diagram, state table and ASM chart for a D flip-flop.
9. Discuss the design procedure of a combinational circuit.
10. Write VHDL code for shift register.

(5 × 5 = 25 marks)

Turn over

Part C

Answer **all** *questions.*

Each full question carries 12 *marks.*

11. Design a combinational circuit using PROM that accepts a 3 bit binary number and generates its equivalent excess 3 code.

Or

12. Realise the functions given below using PAL with four inputs and 3-wide AND-OR structure. Also write PAL programming table :

$F_1 (W, X, Y, Z) = \Sigma m (6, 8, 9, 12 - 15)$.

$F_2 (W, X, Y, Z) = \Sigma m (1, 4 - 7, 10 - 13)$.

$F_3 (W, X, Y, Z) = \Sigma m (4 - 7, 10 - 11)$.

$F_4 (W, X, Y, Z) = \Sigma m (4 - 7, 9 - 15)$.

(12 marks)

13. Write short notes on :

(a) RS 485.

(b) RS 422.

(6 + 6 = 12 marks)

Or

14. Explain the functions and uses of any one bus interface IC. How will you interface the same to the processor ?

(12 marks)

15. (a) Draw the state diagram and state table for a Moore type sequence detector to detect the sequence 110.

(8 marks)

(b) Obtain the state diagram of a mod-6 counter. (4 marks)

Or

16. (a) Explain the steps involved in minimising a finite state machine. (4 marks)

(b) Determine a minimal state table equivalent to the given below table :

PS	NS, Z	
	X = 0,	X = 1
S_1	S_1, 1	S_1, 0
S_2	S_1, 1	S_6, 1
S_3	S_2, 0	S_5, 0
S_4	S_1, 0	S_7, 0
S_5	S_4, 1	S_3, 1
S_6	S_2, 0	S_5, 0
S_7	S_6, 1	S_3, 1

(8 marks)

17. (a) Write a VHDL code to realise a 4 × 1 MUX in Behavioral Modelling. (6 marks)

(b) Write VHDL Code to realise a priority encoder in behavioral modelling. (6 marks)

Or

18. (a) Write VHDL code for design of 3 to 8 decoder using DATA FLOW modelling. (6 marks)

(b) Write VHDL Code for 4 to 1 MUX in structural modelling and draw its waveforms. (6 marks)

19. Write short notes on shift register and write the VHDL code for shift register. (6 + 6 = 12 marks)

Or

20. What are attributes ? Write the VHDL code for implementing a D flip-flop. (12 marks)

[5 × 12 = 60 marks]