Register No.: …… Name: ……..

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

SECOND SEMESTER M.TECH DEGREE EXAMINATION (Regular), JULY 2022

VLSI AND EMBEDDED SYSTEMS

(2021 Scheme)

Course Code: **21VE206-A**

Course Name: **High Speed Digital Design**

Max. Marks: **60** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Comment on the parameters frequency and time of high speed circuits. Determine the reactance of a high speed circuit with a capacitance of 120pF and a resistance of 470 Ω at the rise times 3 ns and 15 ns.
2. Illustrate and explain the electrical model of a CRO probe. Comment on the Q factor of the equivalent circuit.
3. Discuss any three methods by which operating margins can be observed in high speed circuits.
4. Derive the characteristic equation of an ideal high speed transmission line.
5. Illustrate and explain any three mechanical properties of vias.
6. State the five rules that determine connector behavior of high speed circuits.
7. Explain timing margin associated with clock distribution with proper illustrations.
8. Summarize the three power rules applicable to high speed circuits.

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

9. A large bus is connected for the shared memory sub-system of a parallel computer. The bus connects 20 small CPUs any of which may access an 8-bit wide RAM. The bus is implemented using 50Ω controlled impedance traces that are 10 inches long. The bus propagation length is much shorter than the rise time of a gate used. Hence, no terminators are used at the ends of the bus. Each bus driver is able to drive 20 other circuits. The maximum propagation delay of each transceiver is 9 ns and the bus is to be operated at a cycle of 30 ns (33 MHz). Compute the load capacitance on each trace and the drive resistance of the three-state output loads. Compute the rise time of the bus as well as the power dissipation associated with each driver. (6)

OR

10. Using appropriate illustrations and equations, explain the reasons for power dissipation in a high speed digital circuit. (6)

MODULE II

11. Explain rise time and bandwidth of oscilloscope with necessary expressions and figures.

An oscilloscope rated at 310 MHz was purchased and its probe was also rated at 310 MHz. Both specifications are of 3 dB bandwidths. How does this combination affect the rise time of the signal displayed, when the input signal has 2.1 ns rise time? (6)

OR

12. Elaborate on Shop Built 21:1 probe, low inductance ground loop fixtures and embedded fixtures for probing. (6)

MODULE III

13. A semiconductor company built their first prototype of a high speed processor. They used point-to-point wiring to reduce the cost and delay of making PCBs. The prototype has the following specifications:
Gates = 6000, signal nets = 2000, knee frequency = 250 MHz, rise time = 2 ns, speed of operation = 85 ps/in, average net length = 4 in, average wire height above ground = 0.2 in, separation between wires = 0.1 in, wire size = 0.01 in, series resistance = 30 Ω, capacitance = 15 pF, step voltage = 3.7 V.
Using the above information, demonstrate that transmission lines are superior to ordinary point-to-point wiring at high speeds in terms of signal distortion and cross talk. (6)

OR

14. Explain how slowing down of a clock system affects the overall performance of a high speed digital system with special reference to meta-stability in clock distribution. (6)

MODULE IV

15. Compare and contrast the features of low–loss and lossy transmission lines. State the unique properties of lossless transmission lines. (6)

OR

16. Explain skin effect and its mechanics at very high speed with relevant equations and illustrations. (6)

MODULE V

17. Examine end terminations in the following cases (i) Rise time by intuition and calculation (ii) DC Biasing. (6)

OR

18. Discuss capacitance and inductance in vias of high speed ICs. (6)

MODULE VI

19. Elaborate on the design of the set of bypass capacitors used for the uniform distribution of a stable reference voltage in a high frequency digital system. (6)

OR

20. Paraphrase delay adjustments at high frequencies and elaborate on the different types of delays using appropriate illustrations. (6)

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