Register No.: ………………………… Name: ……………………………………………………..

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

THIRD SEMESTER INTEGRATED M.C.A DEGREE EXAMINATION (S), MAY 2022

(2020 SCHEME)

Course Code:	**20IMCAT201**
Course Name:	**Computer Organization**
Max. Marks:	**60**

Duration: 3 Hours

PART A

(Answer all questions. Each question carries 3 marks)

1. Explain subroutines. Analyze the use of call or return instructions in a subroutine.
2. Comment on the basic memory operations.
3. Analyze the working of a single bus organization.
4. Explain the basic organization of hardwired control unit.
5. What is the purpose of a control unit?
6. What is a Fast Adder?
7. Enumerate the features of a universal serial bus.
8. Differentiate parallel port and serial port.
9. Explain the function of a cache memory.
10. Analyze the working mechanism of asynchronous DRAMs.

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

11. With a neat diagram, explain the basic operational concepts of a computer. (6)

OR

12. With suitable examples, explain any four types of addressing modes. (6)

MODULE II

13. Describe the micro-programmed control organization. Compare its advantages over hardwired control. (6)

OR

14. Compare and contrast single bus organization with multiple bus organization. (6)

MODULE III

15. Design a carry look ahead adder and explain its functions. (6)

OR

16. Explain Booth's algorithm in detail. (6)

MODULE IV

17. With a neat sketch, explain the various methods for handling multiple interrupt requests raised by multiple devices.   (6)

OR

18. Explain the various bus arbitration techniques.   (6)

MODULE V

19. Write short note on set-associative mapping function of cache memory.   (6)

OR

20. With a neat diagram, explain the internal organization of 128 X 8 memory chip.   (6)

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