Register No.: …… Name: ……..

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

THIRD SEMESTER M.TECH DEGREE EXAMINATION (Regular), FEBRUARY 2022

(VLSI & Embedded Systems)

(2020 Scheme)

Course Code: **20ECVET213**

Course Name: **High Speed Digital Design**

Max. Marks: **60** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Comment on the parameters frequency and time of high speed circuits. Determine the reactance of a high speed circuit with a capacitance of 150pF and a resistance of 330 Ω at the rise times 5ns and 20ns.
2. Explain any three types of packages employed for high speed ICs.
3. Discuss briefly how operating margins can be observed in high speed circuits.
4. Derive the characteristic impedance of an ideal transmission line at high speeds.
5. Cross talk arises due to mutual inductance in connectors. Substantiate using illustrations and equations.
6. State the five rules that determine connector behavior at high speeds.
7. Explain timing margin associated with clock distribution.
8. Discuss how uniform voltage distribution is ensured with reference to the resistance and inductance of power distribution wiring.

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

9. Using appropriate illustrations and equations, explain the reasons for power dissipation in a high-speed digital circuit. (6)

OR

10. Associate the effect of sudden change in voltage and current with the speed of operation of high-speed digital circuits.
Determine the output resistance of a CMOS driver with the quoted ratings as given below at a power supply voltage of 4.6 V:

V_{OL} at I_O=4 mA (6)
Typical value at 25^0C=0.15 V
Maximum value between -40^0C and 85^0C=0.33 V
V_{OH} at I_O=-4 mA
Typical value at 25^0C=4.30 V
Maximum value between -40^0C and 85^0C=3.85 V

MODULE II

11. With the help of electrical model of oscilloscope, elaborate the estimation of self-inductance of probe ground loop and Q value of the probing circuit.
Compute the LC time constant and thus the 10-90% rise time for a critically damped two-pole circuit given the electrical equivalent of the CRO probe has a self-inductance of 200 nH, shunt capacitance of 10 pF and shunt resistance of 10 MΩ. (6)

OR

12. A signal source is connected through a transmission line of impedance 50Ω connected to a 50Ω terminator. At the terminating end, a sensing probe with a 1000Ω resistor is connected, the other end of which leads to a 50Ω terminated output and then to a high-speed sampling scope. Compute the expected rise time degradation when the probe under test behaves as a simple capacitive load of 10pF. Determine the composite rise time at the probe under test if the signal has a rise time of 600ps. (6)

With the help of proper illustrations and expressions, discuss the rise time and bandwidth of oscilloscope.

MODULE III

13. A semiconductor company built their first prototype of a high-speed processor. They used point-to-point wiring to reduce the cost and delay of making PCBs. The prototype has the following specifications:
Gates = 6000, signal nets = 2000, knee frequency = 250 MHz, rise time = 2 ns, speed of operation = 85 ps/in, average net length = 4 in, average wire height above ground = 0.2 in, separation between wires = 0.1 in, wire size = 0.01 in, series resistance = 30 Ω, capacitance = 15 pF, step voltage = 3.7 V. (6)
Using the above information, demonstrate that transmission lines are superior to ordinary point-to-point wiring at high speeds in terms of signal distortion and cross talk.

OR

14. Paraphrase meta-stability. Discuss, with the help of figures, waveforms and equations, how meta-stability is measured, its causes and how to prevent its occurrence. (6)

MODULE IV

15. Explain in detail skin effect and its mechanics at very high speeds. (6)

OR

16. Interpret lossless transmission lines at high speeds. Compare and contrast between LC and RC transmission lines. (6)

MODULE V

17. Analyze end terminations under the following heads:
    (i) Rise time by intuition and calculation (6)
    (ii) DC biasing

OR

18. Discuss capacitance and inductance in vias of high-speed ICs. (6)

MODULE VI

19. With suitable diagrams, paraphrase the design rules to be followed for providing stable voltage reference to high speed digital systems. (6)

OR

20. Paraphrase clock jitter. Give the reasons for the same. Discuss different methods for measurement of clock jitter. (6)

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