Register No.: …… Name: ……

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

SECOND SEMESTER INTEGRATED MCA DEGREE EXAMINATION (Special), AUGUST 2021

Course Code: **20IMCAT106**

Course Name: **INTRODUCTION TO DIGITAL SYSTEMS & LOGIC DESIGNS**

Max. Marks: **60** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

		CO
1.	Write short note on 1's and 2's Compliment form with examples.	[1]
2.	Covert 101111 and 1001011 to decimal.	[1]
3.	Realize the XOR function using NAR/NOR Logic.	[2]
4.	State and prove distributive laws in Boolean Algebra.	[2]
5.	Differentiate latches and flip flops.	[3]
6.	Describe T-flip flop.	[3]
7.	With a neat diagram illustrate 4x1 multiplexer.	[4]
8.	Illustrate the truth table and logic diagram of a half adder.	[5]
9.	Summarize on asynchronous counters.	[6]
10.	Outline any three applications of shift registers.	[6]

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

		CO	Marks
11.	Summarize on Hexadecimal Number system with example.	[1]	(6)

OR

		CO	Marks
12.	Represent $(115)_{10}$ in 1's complement and 2's complement form.	[1]	(6)

MODULE II

		CO	Marks
13.	Prove the universal properties of NAND gate.	[4]	(6)

OR

		CO	Marks
14.	State and prove De Morgan's theorem. With suitable examples	[2]	(6)

MODULE III

		CO	Marks
15.	Reduce the expression ∑m(0,2,3,4,5,6) using k-map.	[3]	(6)

OR

		CO	Marks
16.	With truth table and logic diagram, explain the working of SR-flip flop.	[5]	(6)

MODULE IV

		CO	Marks
17.	Explain full-subtractor.	[5]	(6)

OR

		CO	Marks
18.	Illustrate the design of decimal to BCD encoder.	[5]	(6)

MODULE V

		CO	Marks
19	Explain a 3-bit binary synchronous counter with logic circuit diagram.	[6]	(6)

OR

		CO	Marks
20.	Design a Parallel-In/Serial-Out register with D-flip-flops.	[6]	(6)

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