Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

SIXTH SEMESTER B.TECH DEGREE EXAMINATION(S), DECEMBER 2019

Course Code: AE308

Course Name: ADVANCED MICROPROCESSORS

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks.

			Marks
1	a)	List the difference between RISC and CISC architecture	(5)
	b)	Explain with neat diagrams the ARM architecture	(10)
2	a)	Compare all ARM processor families	(6)
	b)	Explain the significance of current program status register in ARM	(4)
	c)	What do you mean by load and store architecture in ARM processor?	(5)
3	a)	Explain with figures the three stage pipeline mechanism in ARM7. Also explain how the total execution time gets reduces with pipelining	(10)
	b)	Briefly explain the general purpose registers in ARM	(5)

PART B

Answer any two full questions, each carries 15 marks.

4	a)	List the advantage of thumb instructions in ARM	(5)
	b)	Explain with examples the Move Instructions and Arithmetic Instructions used in ARM	(10)
5	a)	What are the restrictions in thumb modes for ARM register access?	(3)
	b)	What are the basic data types used in C programming?	(4)
	c)	Explain with required flow charts the different looping structures used in C programming	(8)
6	a)	What are the advantages of inline Functions and Inline Assembly?	(7)
	b)	Write a C program for finding the factorial of a number given by a user	(8)

PART C

Answer any two full questions, each carries 20 marks.

7	a)	Explain the purpose of Translation Look aside Buffer	(5)
	b)	How mapping a task in virtual memory to physical memory is done in ARM core?	(8)
	c)	Explain the advantages of cache memory in ARM microcontroller	(7)

8	a)	Explain the concepts of page tables. What is its significance in multiprocessing?	(10)
	b)	List the exceptions and associated modes in ARM processor	(6)
	c)	Which all ARM registers are affected during an exception?	(4)
9	a)	Explain with relevant figures the advanced microprocessor bus architecture bus system.	(15)
	b)	Compare ABH, ASB, APB microcontroller bus architecture.	(5)

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