Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FIFTH SEMESTER B.TECH DEGREE EXAMINATION(R&S), DECEMBER 2019

Course Code: AE363

Course Name: VLSI CIRCUIT DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks. Marks

1 a) With the help of neat diagrams explain NMOS IC process.. (8)

b) Explain different narrow channel effects of MOSFET. (7)

2 a) Draw and explain the operation of an ion implantation system. (4)

b) Compare CMOS technology with BiCMOS technology. (3)

c) Prove that saturation drain current ($I_D$sat.) of MOSFET depends only on gate source voltage V_{GS}. (8)

3 a) Explain GaAs technology with the help of necessary diagrams. (7)

b) With C-V curve explain the capacitance in the accumulation, depletion and inversion region of MOS device. (8)

PART B

Answer any two full questions, each carries 15 marks.

4 a) Implement the Boolean function $y=\overline{(A+B+C)+DEF}$ using CMOS logic and Pseudo NMOS logic. (8)

b) Explain layout design rules for CMOS logic. (5)

c) What are the properties of stick diagrams. (2)

5 a) Draw the circuit of a CMOS inverter and explain its transfer characteristics. (7)

b) Draw the circuit diagram and stick diagram of 2 input CMOS NOR gate. (8)

6 a) List out λ (lambda) based design rules for CMOS technology. (7)

b) Explain Domino logic and np CMOS logic with examples. (8)

PART C

Answer any two full questions, each carries 20 marks.

7 a) Explain constant voltage scaling and its influence on different device parameters. (10)

b) Write short notes on synchronizers. (10)

8 a) Write short notes on Passive& Active bus lines. (5)

	b)	Explain any one method of two phase clock generation.	(5)
	c)	Explain about stack borrowing technique in latch based clocking.	(10)
9	a)	Explain Dual rail coding used to generate completion signal.	(10)
	b)	Explain the impact of clock skew in VLSI system with a neat figure.	(10)

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