APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Scheme for Valuation/Answer Key

Scheme of evaluation (marks in brackets) and answers of problems/key

EIGHTH SEMESTER B.TECH DEGREE EXAMINATION, MAY 2019

Course Code: CS404

Course Name: Embedded Systems

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 4 marks.

		Marks
1	Definition - 2 marks, Any two functionalities -2 marks	(4)
2	Four problems of hardware software co-design	(4x1)
3	Concurrent program model for Seat Belt Warning System	(4)
4	Explanation of the library file in assembly language context (2 marks) Benefit of 'library file'(2 marks)	(4)
5	Out of circuit programming method	(4)
6	Generic IDEs with example- 2 marks, IDEs used in embedded firmware development with example- 2 marks	(2+2)
7	Hard real time consideration (2 marks) and soft real time consideration (2 marks)	(2+ 2)
8	Monolithic kernel - Any two valid points (2 Marks) Micro kernel - Any two valid points (2 Marks)	(4)
9	Definition or concept of SOC - 2 Marks.Any two additional valid points about SOC like advantage, area of application, example, etc. - 2 Marks.	(4)
10	Any 4 bottlenecks	(4 x 1)

PART B

Answer any two full questions, each carries 9 marks.

11	a)	General explanation of specification phase (Any three valid points) - 3 Marks . Example - 2 Marks	(5)
	b)	UML representation of Objects and Classes - 2 marks each	(4)
12		States and Diagram in correct sequences	(9)
13	a)	Any four non functional requirements in an embedded system	(4)
	b)	Relevant classes & their representations using rectangle : 2 Marks Relevant attributes : 1 Mark Relevant methods : 1 Mark Relevant relationships between classes : 1 Mark	(5)

PART C

Answer any two full questions, each carries 9 marks.

14		Diagram - 3 Marks. Explanation of steps in converting assembly language to machine language - 6 Marks	(9)
15	(a)	Explanation	(5)
	(b)	Explanation	(4)
16	a)	Yes -1 mark, Use of factory programmed chip- 2 marks	(3)
	b)	merits + demerits of assembly language	(3+ 3)

PART D

Answer any two full questions, each carries 12 marks.

17		Different types of Inter Task Communication mechanisms	(3x4)
18	a)	Diagram(1 mark) Explain the various steps (4 marks)	(5)
	b)	Need + Explanation of reengineering	(3+1)
	c)	Any 3 factors	(3)
19	a)	Two-level ISR Handling : RTOS First Interrupts, Calls to corresponding ISR, then ISR sending messages to Interrupt Service Threads Diagram : 2 Marks Explanation of 8 Steps : 4 Marks Since this is an analytical question. Any type of interrupt handling can be granted marks if the student is able to justify.	(3 + 3)
	b)	Listing names of four types of testing - 2 Marks Definition of four types of testing - 1 Mark each	(3x3)

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