Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

SECOND SEMESTER REGULAR M.C.A. DEGREE EXAMINATION(R&S), MAY 2019

Course Code: RLMCA112

Course Name: COMPUTER ORGANIZATION AND ARCHITECTURE

Max. Marks: 60 Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks. Marks

1	Distinguish between system software and application software.	(3)
2	Discuss the use of stack in subroutines.	(3)
3	Write the control sequence to execute the instruction Add (R3),R1 using single bus organization.	(3)
4	Explain the need for WMFC signal when reading from or writing to main memory?	(3)
5	Explain uses of interrupt vector in handling interrupts.	(3)
6	Explain the working of SRAM cell.	(3)
7	Define cache memory. Explain cache hit and cache miss.	(3)
8	What is memory interleaving? What are the advantages of interleaving the memory?	(3)

PART B

Answer any one question from each module. Each question carries 6 marks.

Module I

9	Explain various types of instruction. Explain the execution of (A+B) ∗ (C+D).	(6)

OR

10	Describe the execution of branch instructions in a computer.	(6)

Module II

11	Discuss the advantage of subroutine. Explain how nested subroutines are executed.	(6)

OR

12	Explain the different addressing modes with examples.	(6)

Module III

13 Draw the block diagram and explain Microprogrammed Control Unit. (6)

OR

14 With neat diagram and suitable example, describe the working of a single bus organization. Explain the advantages and disadvantages of single bus organization. (6)

Module IV

15 Discuss the working of USB standard I/O interface. (6)

OR

16 Describe the I/O data transfer mechanism using DMA. (6)

Module V

17 Compare and contrast DRAM and SDRAM with block diagrams. (6)

OR

18 Explain the internal organization of a dynamic memory chip and design 1K* 8 memory chip using decoders. (6)

Module VI

19 Discuss the virtual memory technique using segmentation with neat diagram. (6)

OR

20 Describe different mapping techniques for cache memory. (6)

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