Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

SEVENTH SEMESTER B.TECH DEGREE EXAMINATION(S), MAY 2019

Course Code: CS405

Course Name: COMPUTER SYSTEM ARCHITECTURE

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 4 marks. Marks

1		With proper equations, explain the terms (i) CPU Time (ii) Throughput Rate	(4)
2		Explain NUMA model for Multiprocessor Systems	(4)
3		Explain the property of locality of reference in memory.	(4)
4		A generalized multiprocessor system architecture combines features from the UMA, NUMA and COMA models. Justify the answer.	(4)
5		Differentiate write-invalidate and write-update coherence protocols for write through caches.	(4)
6		Explain the factors speedup, efficiency and throughput of a k-stage linear pipeline.	(4)
7		Illustrate with example how internal data forwarding among multiple functional units can improve the throughput of a pipelined processor.	(4)
8		With an example bring out the difference between the Carry-Save Adders (CSA) and Carry Propagate Adder (CPA).	(4)
9		Explain the distributed cacheing.	(4)
10		Illustrate the scalable coherence interface (SCI) interconnect model.	(4)

PART B

Answer any two full questions, each carries 9 marks.

11	a)	What is the significance of Bernstein's conditions to detect parallelism?	(4)
	b)	Consider the execution of the following code segment consisting of seven statements. Use Bernstein's conditions to detect the maximum parallelism embedded in this code. Justify the portions that can be executed in parallel and the remaining portions that must be executed sequentially. Rewrite the code using parallel constructs such as Cobegin and Coend. No variable substitution is allowed. All statements can be executed in parallel if they are declared within the same block of a (Cobegin and Coend) pair.	

S1: A=B+C

S2: C=D+E

S3: F=G+E

S4: C=A+F

S5: M=G+C

S6: A=L+E

S7: A=E+A (5)

12 a) Explain memory hierarchy. (3)

b) You are asked to perform capacity planning for a two-level memory system. The first level, M_1, is a cache with three capacity choices of 64 Kbytes, 128 Kbytes, and 256 Kbytes. The second level, M_2, is a main memory with a 4-Mbyte capacity. Let c_1 and c_2 be the cost per byte and t_1 and t_2 the access times for M_1 and M_2 respectively. Assume $c_1=20c_2$ and $t_2=10t_1$. The cache hit ratios for the three capacities are assumed to be 0.7, 0.9 and 0.98 respectively.

(i) What is the average access time t_a in terms of t_1=20 ns in the three cache designs? (Note that t_1 is the time form CPU to M_1 and t_2 is that from CPU to M_2)

(ii) Express the average byte cost of the entire memory hierarchy if c_2=$0.2/Kbyte. (6)

13 a) Explain SIMD machine model. (3)

b) Explain Superscalar architecture. Also explain pipelining in superscalar processors. (6)

PART C

Answer any two full questions, each carries 9 marks.

14 a) Explain hot spot problem. (3)

b) Design an 8 input omega network using 2X2 switches as building blocks. Show the switch settings for the permutations π_1=(0,7,6,4,2)(1,3)(5). Show the conflicts in switch settings, if any. Explain blocking and non-blocking networks in this context. (6)

15 a) Differentiate between linear and nonlinear pipeline processor. (3)

b) Consider the following pipeline reservation table:.

	1	2	3	4	5	6
S1	X					X
S2		X			X	
S3			X			
S4				X		
S5		X				X

i) What are the forbidden latencies?

ii) Draw the transition diagram.

iii) List all the simple cycles and greedy cycles.

iv) Determine the optimal constant latency cycle and minimal average latency (MAL)

v) Let he pipeline clock period be τ=20ns. Determine the throughput of the pipeline. (6)

16 a) Explain write- invalidate snoopy protocol using write back policy. (4)

b) Explain various message routing schemes used in message passing multi-computers. (5)

PART D

Answer any two full questions, each carries 12 marks.

17 a) Explain in detail the effect of branching and various branch handling strategies. (9)

b) Explain the scoreboarding scheme employed by the CDC 6600 processor. (3)

18 a) With a neat diagram explain the architecture of a multiple context processor model. (6)

b) What are the problems of asynchrony and their solutions in massively parallel processors? (6)

19 a) Compare the design and performance of a superpipelined and superpipelined superscalar processors. (6)

b) With a neat diagram explain the MIT/Motorola *T prototype multithreaded architecture. (6)

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