Reg No.:_____   Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
FIFTH SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018
Course Code: EC361
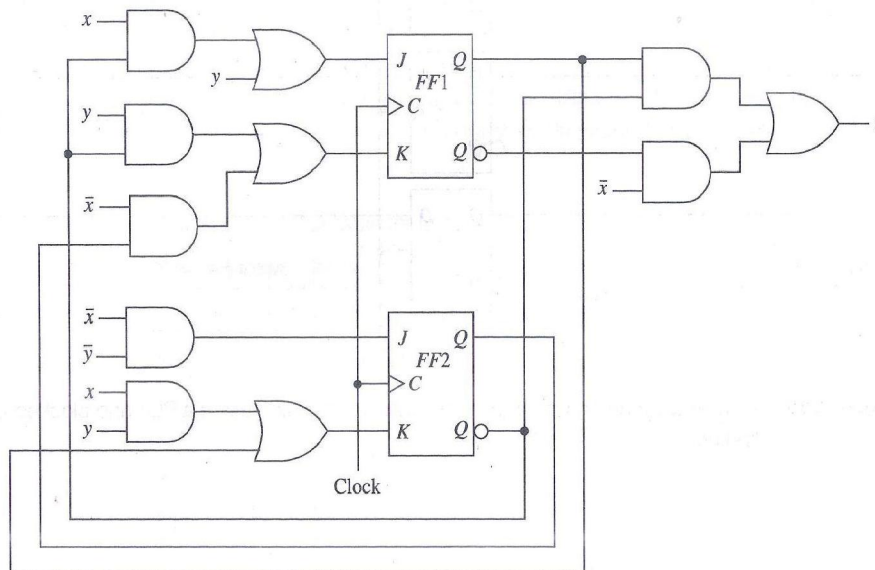**Course Name: DIGITAL SYSTEM DESIGN**

Max. Marks: 100   Duration: 3 Hours

PART A
Answer any two full questions, each carries 15 marks.   Marks

1 a) Analyse the following clocked synchronous sequential network. Derive the next   (9)
       state and output equations. Obtain the excitation table, transition table, state table
       and state diagram.

   b) Construct an ASM chart for a sequence recognizer to recognize the input sequence   (6)
       of pairs $x_1x_2 = 01, 01, 11, 00$. The output variable 'z' is asserted when $x_1x_2 = 00$, if
       and only if the three preceding pairs of inputs are $x_1x_2 = 01, 01$ and 11, in that
       order.

2 a) Analyze the asynchronous sequential network by forming the excitation/transition   (9)
       table, state table, flow table and flow diagram. The network operates in the
       fundamental mode with the restriction that only one input variable can change at a
       time.
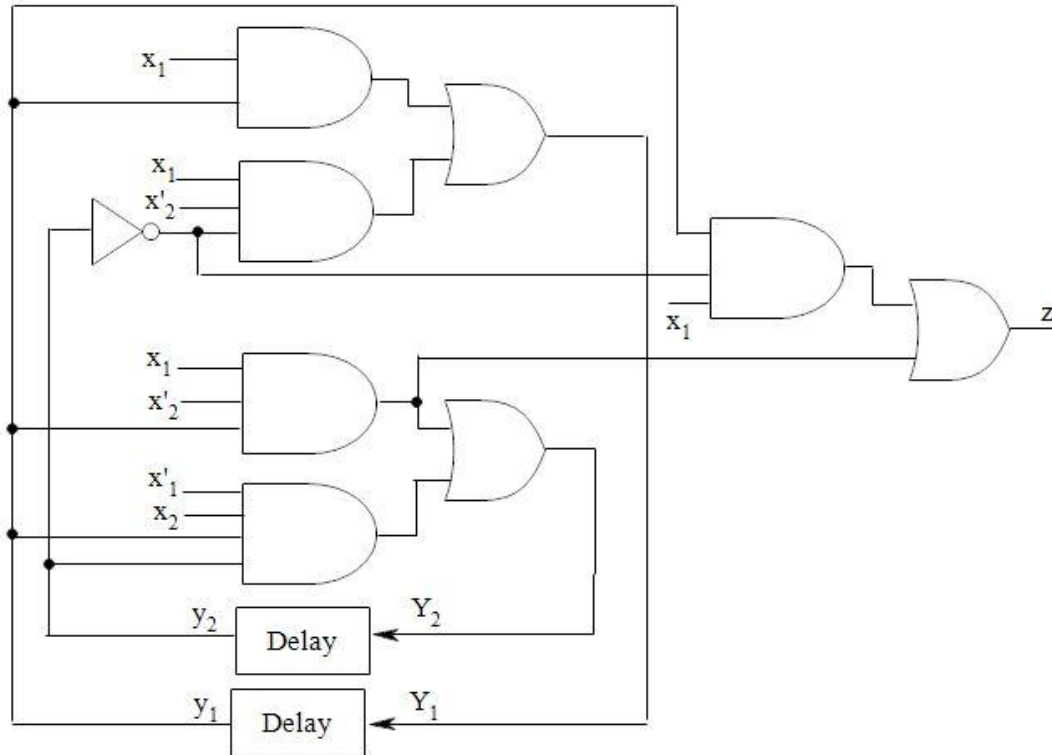
b) A reduced flow table for a fundamental-mode asynchronous sequential network is   (6)
given below. Using the universal multiple-row state assignment, construct the
corresponding expanded flow table and transition table. Assign outputs where
necessary such that there is at most a single output change during the time the
network is unstable. Assume that the inputs x_1 and x_2 never change
simultaneously.

Present state	Next state				Output (z)			
	Input state ($x_1 x_2$)				Input state ($x_1 x_2$)			
	00	01	10	11	00	01	10	11
A	Ⓐ	B	Ⓐ	D	1	-	0	-
B	D	Ⓑ	Ⓑ	C	-	0	1	-
C	A	Ⓒ	Ⓒ	Ⓒ	-	1	1	0
D	Ⓓ	C	A	Ⓓ	0	-	-	1

3 a) Obtain a minimal state table for a clocked synchronous sequential network having   (7)
a single input line 'x' in which the symbols 0 and 1 are applied and a single output
line 'z'. An output of 1 is to be produced if and only if the 3 input symbols
following two consecutive input 0's consist of at least one 1. An example of
input/output sequences that satisfy the conditions of the network specifications is:

     x= 010001001001001000000000011

     z= 000000100000010000000000001

b) Construct an ASM chart for the following state diagram shown. Determine the model of CSSN that this system conforms to with proper justification.   (5)
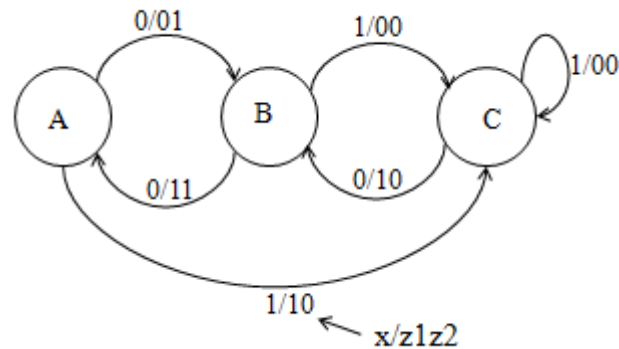
c) Explain races in ASC with example.   (3)

PART B
Answer any two full questions, each carries 15 marks.

4 a) Examine the possibility of hazard in the OR-AND logic circuit whose Boolean function is given by $f = \Sigma(0,2,6,7)$. Show how the hazard can be detected and eliminated.   (7)

b) Discuss the concept of switch bouncing and suggest a suitable solution.   (4)

c) Explain essential hazards in asynchronous sequential networks.   (4)

5 a) Illustrate the fault table method used for effective test set generation for the circuit whose Boolean function is $z = \overline{x_1}x_2 + x_3$ (7)

b) Find the test vectors of all SA0 and SA1 faults of the circuit whose Boolean function is $f = \bar{x}_1 x_2 + x_1 x_2 x_3$ by the Kohavi algorithm.   (8)

6 a) What is jitter? List the sources of clock jitter.   (5)

b) Describe the operation of Mixed Operating Mode asynchronous sequential circuit.   (4)

c) Write a note on BIST techniques.   (6)

PART C
Answer any two full questions, each carries 20 marks.

7 a) Explain the different kinds of PLA folding.   (10)

b) Draw and explain the architecture of Xilinx XC4000 configurable logic block.   (10)

8 a) Draw and explain the architecture of Xilinx 9500 CPLD family. Also explain the function block architecture.   (10)

b) Explain different testable PLA designs.   (10)

9 a) Using a suitable example, illustrate the fault models in PLA.   (10)

b) Explain the internal structure of XC4000 input/output block.   (10)

****