		CS203-DETAILED-SCHEME	Total Pages:

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
THIRD SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018

Course Code: CS203

Course Name: **SWITCHING THEORY AND LOGIC DESIGN**

Max. Marks: **100** | Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks. | Marks

1 **Find the 9's and 10's complement of $(24579.12)_{10}$.** (3)

(9's complement -1.5 marks   10's complement -1.5 marks)

9's complement

$$\begin{array}{r} 99999.99- \\ \underline{24579.12} \\ 75420.87 \end{array}$$

10's complement

9's complement + 0.01=75420.88

By definition, 10's complement is 10^n- N and 9's complement is 10^n - 10^-m - N where n and m are number of digits in the integer and fractional part and N is the given number.
Thus 10's complement is 100000-25479.12 and 9's complement is 100000-1/100-24579.12

2 **Convert $(455)_{10}$ to base-4,8 and 16.** (3)

(1 mark each for each conversion)

*Number 455 (base 10) is in base 4**: 13013***

*Number 455 (base 10) is in base 8**: 707.***

*Number 455 (base 10) is in base 16: **1c7.***

3 **Express the following functions as product of max-terms:** (3)

a) F(X,Y,Z) = Y' +XZ' + XY'Z'   b) F(A,B,C) = C (A+B') (A' +B' + C')

(1.5 marks, 1.5 marks)

a) $F(X,Y,Z) = Y' + XZ' + XY'Z'$
$= 000+001+100+101+110$
$= \sum m(0,1,4,5,6)$
$= \pi_M (2,3\,7) = (X+Y'+Z)(X+Y'+Z')(X'+Y'+Z')$

b) $F(A,B,C) = C(A+B')(A'+B'+C') = A'B'C + AB'C = = \sum m(1,5)$
$= \pi_M (0,2,4,6,3,7)$

Complete algebraic expansion using OR distributed over AND may also be accepted.

4 **Use Boolean Algebra to show that A'BC'+AB'C'+AB'C+ABC'+ ABC = A+BC'**

(Proof using postulates and theorems)

$A'BC' + AB'C' + AB'C + ABC' + ABC$
$= A'BC' + AB'(C'+C) + AB(C'+C)$
$= A'BC' + AB' + AB$
$= A'BC' + A(B'+B)$
$= (A+A')(A+'BC')$
$= A+'BC'$

PART B

Answer any two full questions, each carries 9 marks.

5 **Simplify F(A,B,C,D)=Σ(1,4,6,7,8,9,10,11,15) using Tabulation method and determine the prime implicants, essential prime implicants and the minimized Boolean expression.** (9)

(Tabulation steps - 5 marks Prime implicants-1 marks essential prime implicant- 2 marks , Minimized Boolean expression-1 marks)

1	0001	1,9	-001		
4	0100	4,6	01-0		
8	1000	8,9	100-		
		8,10	10-0		
6	0110				
9	1001	6,7	011-	8,9,10,11	10--
10	1010	9,11	10-1	8,9,10,11	10--
		10,11	101-		
7	0111				
11	1011	7,15	-111		
		11.15	1-11		
15	1111				

Prime implicants: B'C'D, A'BD', A'BC, BCD, ACD, AB'

	1	4	6	7	8	9	10	11	15
AB'					X	X	X	X	
B'C'D	X					X			
A'BD'		X	X						
A'BC			X	X					
BCD				X					X
ACD								X	X
	√	√	√		√	√	√	√	

Essential Prime Implicants: BCD , A'BD' , B'C'D , AB'

Minimized Boolean expression: BCD+A'BD'+B'C'D+AB'

6 **a)** **Subtract $(9F2C)_{16}$ from $(A96B)_{16}$ using 15's and 16's complement method.** (4)

(Each method- 2 marks.)

Answer :A3F

15's complement of 9F2C is =60D3

A96B+60D3=10A3E 0A3E+1 = 0A3F or A3F

16's complement of 9F2C is =60D4

A96B+60D4=10A3F Answer is 0A3F or A3F

b) **Subtract 366 from 170 in BCD using 10's complement addition.** (3)

(BCD using 10's complement addition)

10's complement of 366 = 634

Adding in BCD

0001 0111 0000
0110 0011 0100
0111 1010 0100
0110
1000 0000 0100

Since there is no carry the result is negative and is the complement of 1000 0000 0100, ie. –0001 1001 0110, that is – 196.

c) **Perform $(417)_8 - (232)_8$ using *8's complement addition*.** (2)

(8's complement addition)

8's complement of **232**

7's complement =777-232=545

8's complement =545+1=546

$(417)_8 - (232)_8$ =417+546=1165

7 a) **Using K-map simplify the Boolean function F as Sum of Products using the don't care conditions d.** (4)

F(w,x,y,z)=w'(x'y+ x'y' +xyz) + x'z'(y+w) d(w,x,y,z)=w'x(y'z + yz) +wyz

(K-map grouping – 2 marks simplification-2 marks)

(Note: one minterm appears is the don'tcare also. The solution below is for both- with and without the don't care minterm included..

	y'z'	y'z	yz	yz'
w'x'	1	1	1	1
w'x		x	1	
wx			1	
wx'	1		x	1

Solution:- w'x'+yz+x'z'

	y'z'	y'z	yz	yz'
w'x'	1	1	1	1
w'x		x	x	
wx			x	
wx'	1		x	1

Solution:- w'x'+x'z'

b) **Represent the following decimal numbers in signed 2's complement 8-bit numbers: i) +43 ii) –19** (3)

(i) +43 - 1 mark ii) –19 - 2 marks)

*(i) +43 =**0010 1011***

ii) –19 =

Binary equivalent of 19 =0001 0011

1's complement =1110 1100

2's complement =1110 1101

c) **Convert the decimal number 3.248 x 10 4 to IEEE 754 standard single precision floating point binary number.** (2)

(IEEE 754 format- 2 mark Any other valid format-1 mark.)

<u>Single Precision frame format (32 bit)</u>

Sign (1 bit)	Exponent (8 bit)	Fractional (23 bit)

1.11111011100000x2^{14} exponent =141

Here,

S=0 (+ve number)

E=10001101
F=11111011100000

0	*10001101*	*11111011100000000000000*

PART C

Answer all questions, each carries 3 marks.

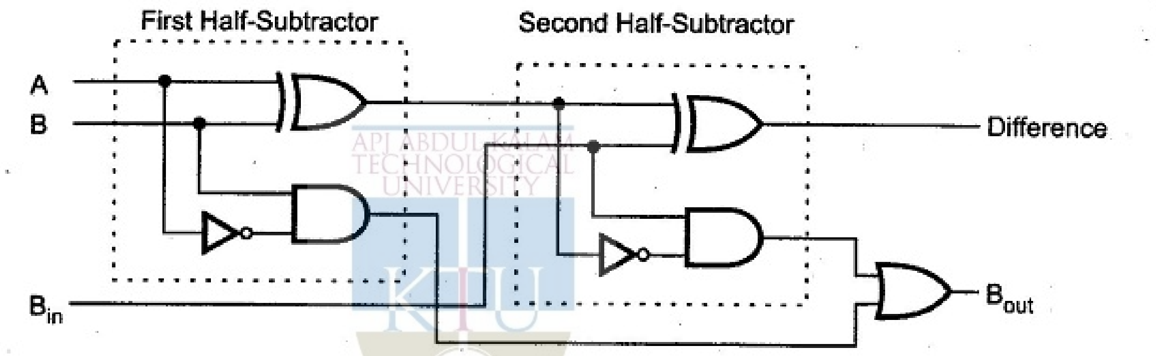
8 **Differentiate combinational and sequential circuits** (3)

(Min 3 differences- 1 mark each)

Combinational	*Sequential*
Output depends only on present input	*Output depends on present input and previous output*
No memory unit	*Memory unit required*
Faster	*Slower*

9 **Given the block diagram of half-subtractor, implement a full-subtractor using half-subtractors.** (3)

(2 half subtractors and OR gate- 3 mark)



10 **Write the excitation tables of SR, JK and T flip-flops.** (3)

(Excitation tables of SR, JK and T flip-flops- 1 mark each)

Excitation table of SR FF

Qn (PS)	*Qn+1 (NS)*	*S*	*R*
0	*0*	*0*	*X*
0	*1*	*1*	*0*
1	*0*	*0*	*1*
1	*1*	*X*	*0*

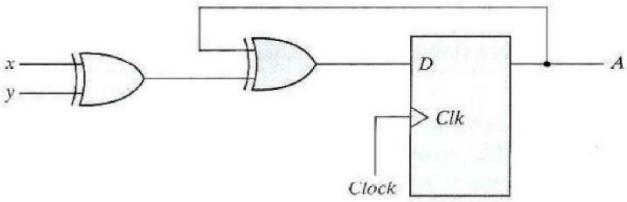
Excitation table of JK FF

Qn (PS)	*Qn+1 (NS)*	*J*	*K*
0	*0*	*0*	*X*
0	*1*	*1*	*X*
1	*0*	*X*	*1*
1	*1*	*X*	*0*

Excitation table of T FF

Qn (PS)	*Qn+1 (NS)*	*T*
0	*0*	*0*
0	*1*	*1*
1	*0*	*1*
1	*1*	*0*

11 **Given below is a sequential circuit using D flip-flop. Write the state table and draw a state diagram.** (3)



(State table – 2 mark State diagram- 1 mark)

Step 1 : Find out input Equation

$D_A = x \oplus y \oplus A$

[2 Mark]

Step 2 : State Table

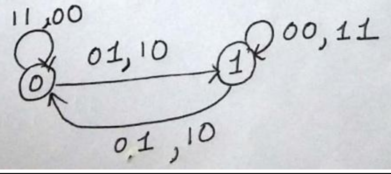
Here $Q_A = A$

Q_A^+ is NS.

PS			input	NS
Q_A	x	y	D_A	Q_A^+
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

[1 Mark]

Step 3 : State Diagram



PART D

Answer any two full questions, each carries 9 marks.

12 **a)** **Design a sequential circuit with JK Flip flops to satisfy the following state equation.** (5)

A(t+1)=A’B’CD + A’B’C + ACD + AC’D’ B(t+1)= A’C + CD’ + A’BC’ C(t+1)= B D(t+1)=D’
(Full design – 5 marks)

FF-A

$$A(t+1) = A'B'CD + A'B'C + ACD + AC'D'$$
$$= A'[B'CD + B'C] + A[CD + C'D']$$
$$= J_A A' + K_A' A$$
$$J_A = B'CD + B'C = B'C$$
$$K_A' = [CD + C'D'] = C'D + CD' \quad \overline{C \oplus D}$$
$$\boxed{K_A = CD + C'D' = (C \oplus D) \quad J_A = B'C}$$

FF-B

$$B(t+1) = A'C + CD' + A'BC'$$
$$= B[A'C'] + (A'C + CD')(B + B')$$
$$= BA'C + CD'B + BA'C' + A'CB' + CD'B'$$
$$= B'[A'C + CD'] + B[A'C + CD' + A'C' + A'C]$$
$$J_B = A'C + CD'$$
$$K_B = [A'C + CD' + A'C']' = (A' + CD')'$$
$$= A \cdot \overline{CD'} = A\overline{C} + AD$$
$$\boxed{J_B = A'C + CD' \quad K_B = A\overline{C} + AD}$$

FF-C

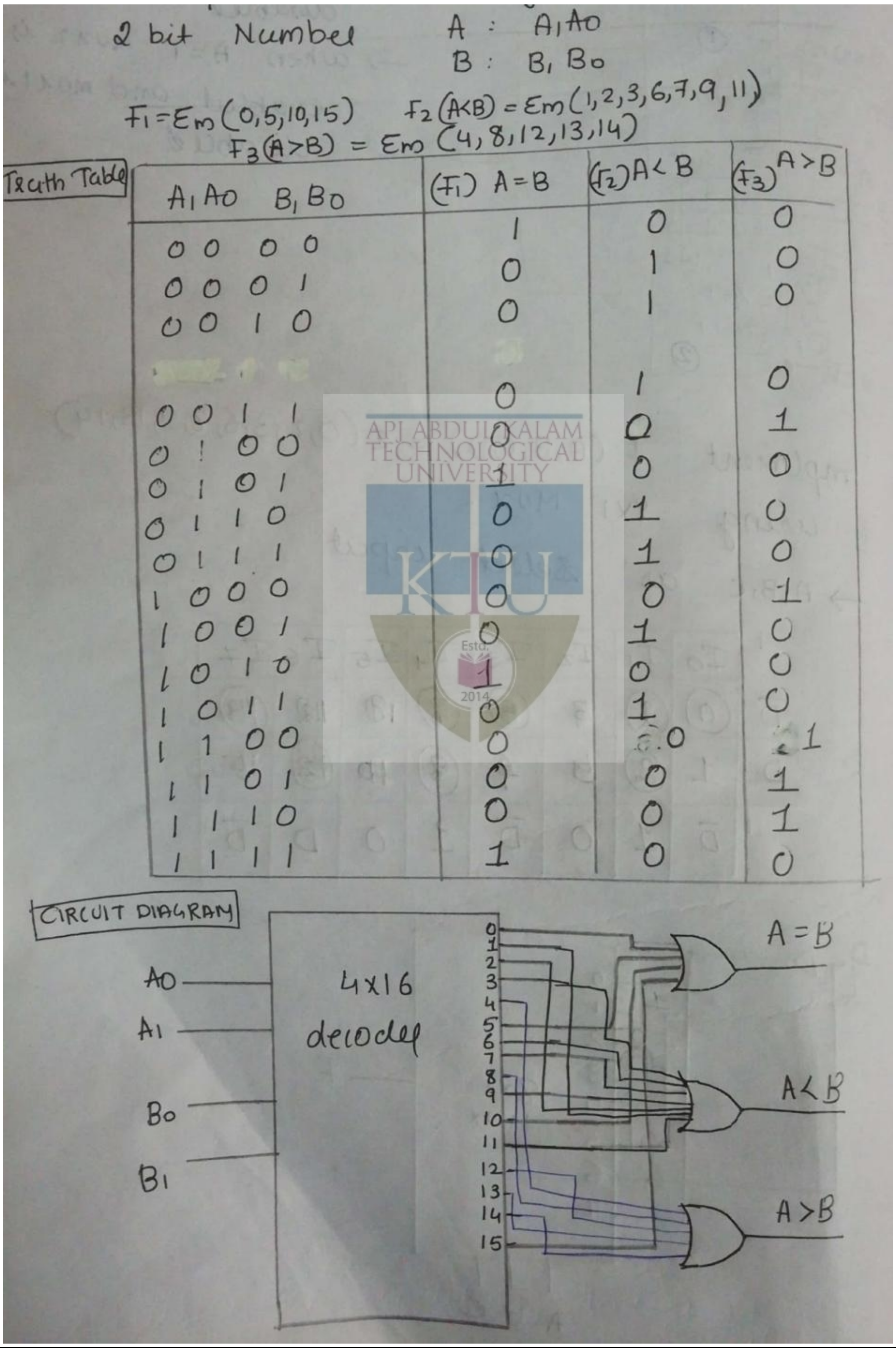
$$C(t+1) = B$$
$$= B(C + C') = BC + BC'$$
$$\boxed{J_C = B \quad K_C = \overline{B}}$$

FF-D

$$D(t+1) = D'$$
$$= 1 \cdot D' + 0 \cdot D$$
$$\boxed{J_D = K_D = 1}$$

		Draw the Circuit diagram using 4 FF based on above equations	

	b)	**Design and implement a decoder that decodes BCD digits (0000 to 1001).** *(Design- 2 marks Implementation- 2 marks)* *Answer : 4 line to 10 line decoder*	(4)
13	**a)**	**Design and implement a 2-bit magnitude comparator using 4X16 decoder.** *(Design – 3 marks Implementation -2 marks.)*	(5)

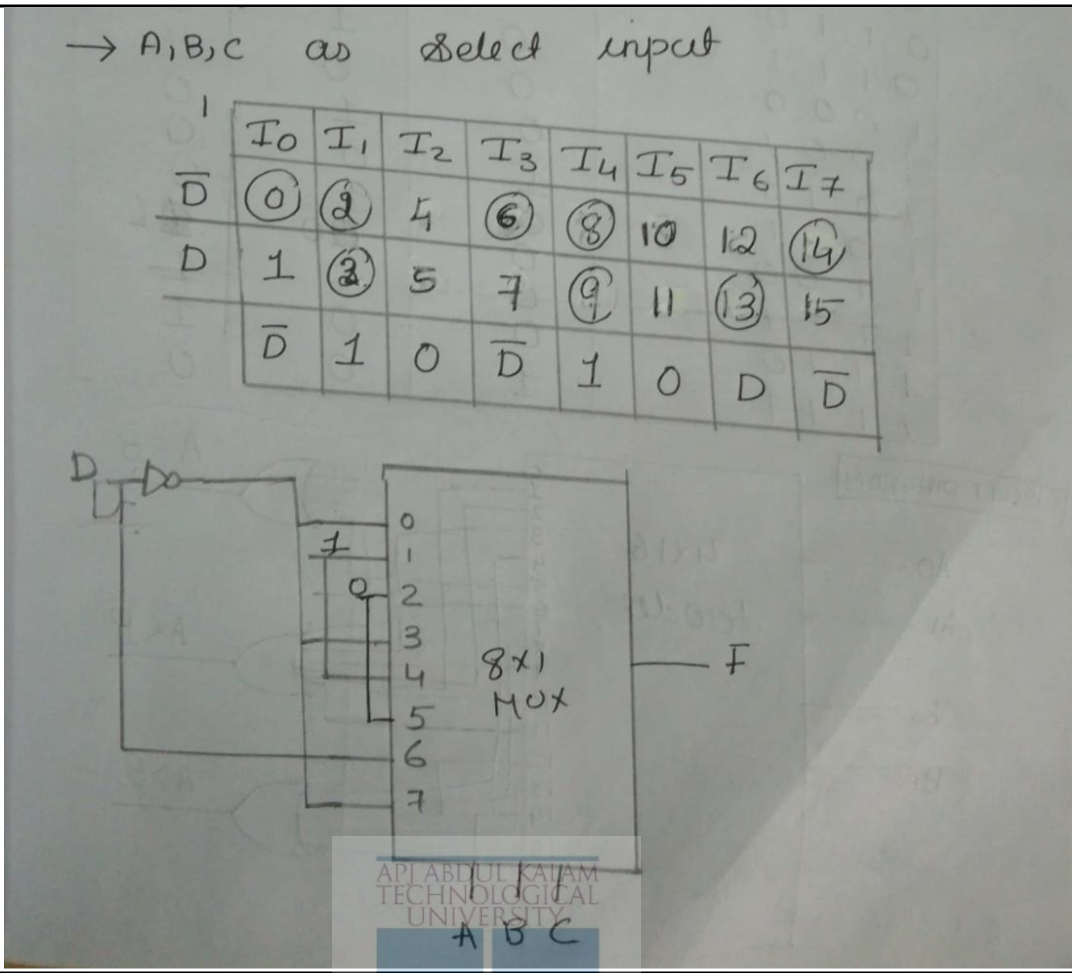

2 bit Number A : A1 A0 B : B1 B0

F1 = Σm (0,5,10,15) F2 (A<B) = Σm (1,2,3,6,7,9,11)
F3 (A>B) = Σm (4,8,12,13,14)

Truth Table

A1 A0	B1 B0	(F1) A=B	(F2) A<B	(F3) A>B
0 0	0 0	1	0	0
0 0	0 1	0	1	0
0 0	1 0	0	1	0
0 0	1 1	0	1	0
0 1	0 0	0	0	1
0 1	0 1	1	0	0
0 1	1 0	0	1	0
0 1	1 1	0	1	0
1 0	0 0	0	0	1
1 0	0 1	0	1	0
1 0	1 0	1	0	0
1 0	1 1	0	1	0
1 1	0 0	0	0	1
1 1	0 1	0	0	1
1 1	1 0	0	0	1
1 1	1 1	1	0	0

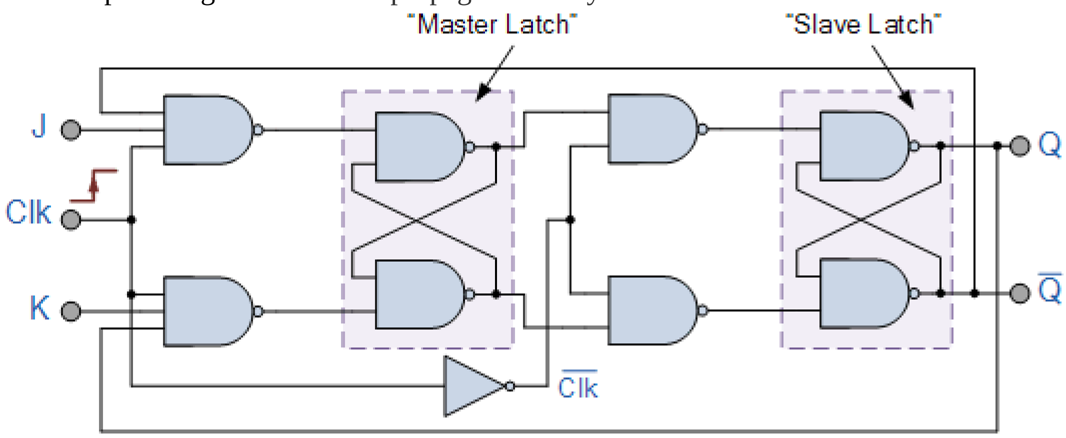
	b)	**Implement f(A,B,C,D)= Σ(0,2,3,6,8,9,13,14) using 8 x 1 MUX .** *(Design using 8 x 1 MUX -4 marks)*	(4)



14		**What is race around condition? Why does it occur? Discuss how master-slave flip-flop eliminates it.**	(9)

(Race around condition-2 marks Reason for Occurrence- 2 marks. Master-slave flip-flop working- 3 marks Diagram – 2 marks .)

In JK Flipflop if J=K=1 the output will oscillate back and forth between 0 and 1 ie there is uncertainity in output at the end of clock pulse. This is race around condition. It occurs as the period of clock pulse is greater than the propagation delay

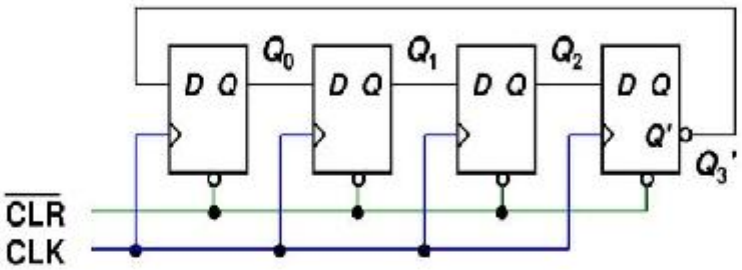


For Block diagram also marks can be given

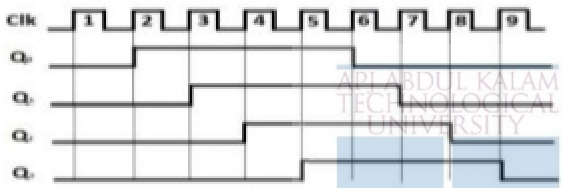
PART E

Answer any four full questions, each carries 10 marks.

15	a)	**Draw the logic diagram of a 4-bit Johnson counter and explain the working with a timing diagram.** *(Logic diagram of a 4-bit Johnson counter -3 marks Working- 2 marks Timing diagram- 3 marks)*	(8)



Clock	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1



b) **Compare Ring counter and Johnson counter.** (2)

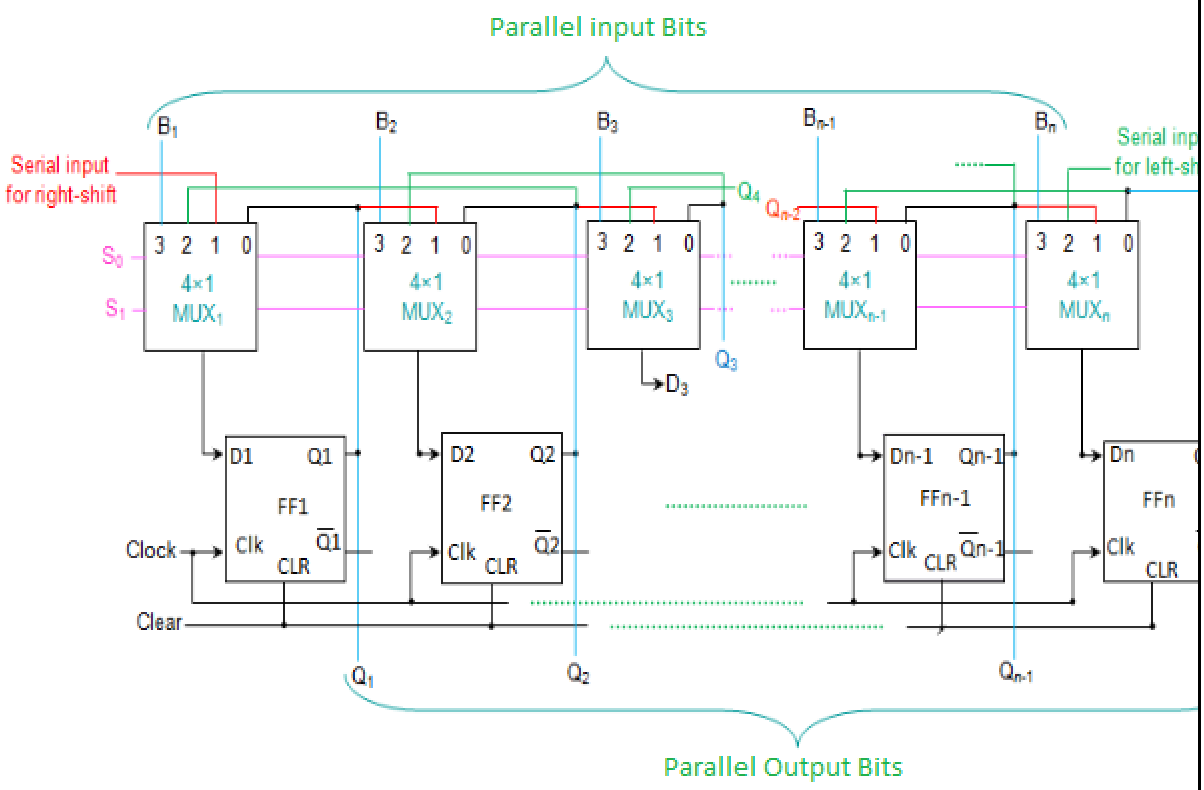
(Any 2 differences- 1 mark each)

Ring	*Johnson*
Output Q of last flipflop given as input to first flipflop	*Output Q' of last flipflop given as input to first flipflop*
Divide by N counter	*Divide by 2N counter*

16 **a)** **Explain the working of 3-bit Universal Shift Register.** (8)

(Working of 3-bit Universal Shift Register-4 marks. Diagram- 4 marks)

N=n-



N=3 In diagram 3 fliflops are only required.

Function table

S1	*S0*	*Reg Operations*
0	*0*	*No change*
0	*1*	*Shift right*
1	*0*	*Shift left*
1	*1*	*Parallel load*

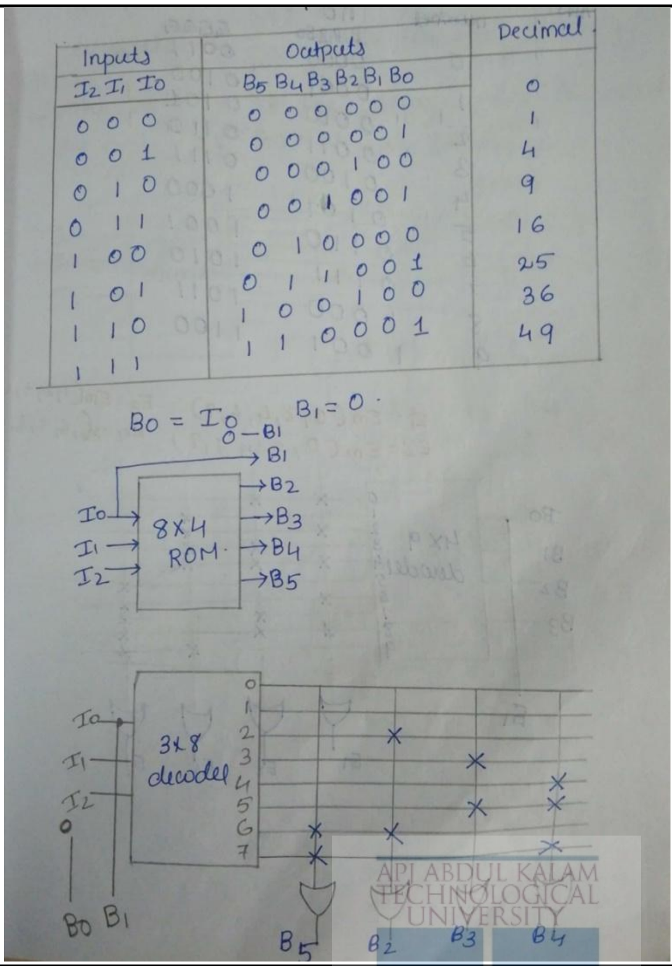
b) **Give 2 applications of shift register.** (2)

(Any 2 applications of shift register- 1 mark each)

1. *Time Delays*
2. *Serial /Parallel data conversion*
3. *Ring counter*
4. *Johnson Counter*
5. *Universal asynchronous receiver transmitter (UART)*
6. *Adder*

17 **a)** **Design a combinational circuit using ROM that accepts a 3-bit binary number and generates output equal to the square of the input number. Use decoder of suitable size to implement ROM.** (7)

(Truth table – 3 marks Rom using decoder – 4 marks)



Inputs $I_2\ I_1\ I_0$	Outputs $B_5\ B_4\ B_3\ B_2\ B_1\ B_0$	Decimal
0 0 0	0 0 0 0 0 0	0
0 0 1	0 0 0 0 0 1	1
0 1 0	0 0 0 1 0 0	4
0 1 1	0 0 1 0 0 1	9
1 0 0	0 1 0 0 0 0	16
1 0 1	0 1 1 0 0 1	25
1 1 0	1 0 0 1 0 0	36
1 1 1	1 1 0 0 0 1	49

$B_0 = I_0$ $B_1 = 0$.

b) **What size of ROM would it take to implement**
i. A BCD adder/subtractor with a control input to select between the addition and subtraction.
ii. A binary multiplier that multiplies two 4-bit numbers.
iii. Dual 4-line to 1-line multiplexers with common selection inputs. (3)

(1 mark each)

i)1024 x 5

ii)256 x 8

iii)1024 x 2

18 **a)** **Design a synchronous counter using JK flip-flops to count the sequence 0,5,6,7,3,2 and then repeats.** (10)

(State table – 2 marks Design using K-map- 6 marks Diagram- 2 marks)

State table

Present state			Next state			Flipflop inputs					
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	J_0	K_0	J_1	K_1	J_2	K_2
0	0	0	1	0	1	1	X	0	X	1	X
1	0	1	1	1	0	X	1	1	X	X	0
1	1	0	1	1	1	1	X	X	0	X	0
1	1	1	0	1	1	X	0	X	0	X	1
0	1	1	0	1	0	X	1	X	0	0	X
0	1	0	0	0	0	0	X	X	1	0	X

Q_2 \ Q_1Q_0	00	01	11	10
0	1	X	X	0
1	X	X	X	1

$J_0 = Q_2 + \overline{Q_1}$

Q_2 \ Q_1Q_0	00	01	11	10
0	X	X	1	X
1	X	1	0	X

$K_0 = \overline{Q_2} + \overline{Q_1}$

Q_2 \ Q_1Q_0	00	01	11	10
0	0	X	X	X
1	X	1	X	X

$J_1 = Q_2$

Q_2 \ Q_1Q_0	00	01	11	10
0	X	X	0	1
1	X	X	0	0

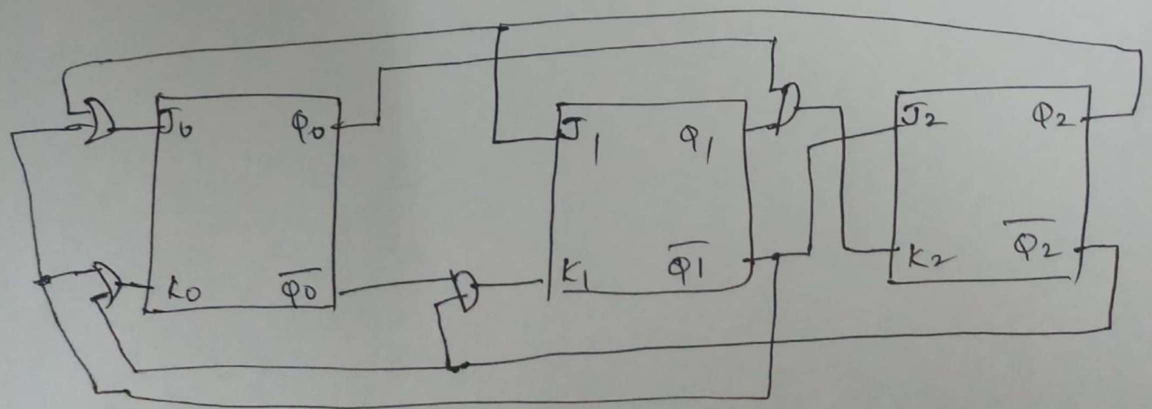
$K_1 = \overline{Q_2}\,\overline{Q_0}$

Q_2 \ Q_1Q_0	00	01	11	10
0	1	X	0	0
1	X	X	X	X

$J_2 = \overline{Q_1}$

Q_2 \ Q_1Q_0	00	01	11	10
0	X	X	X	X
1	X	0	1	0

$K_2 = Q_1 Q_0$

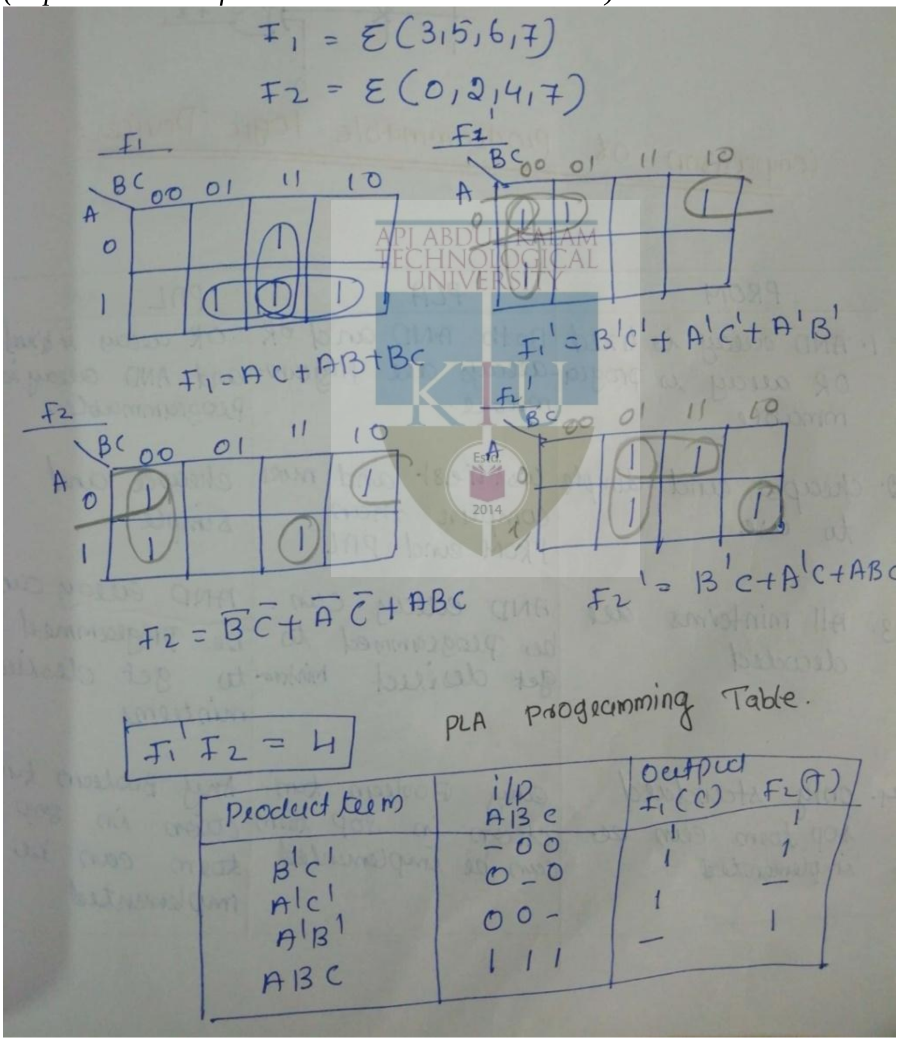


19	**a)**	**Compare static and dynamic RAMs.** *(3 differences- 1 mark each)*	(3)

Static RAM	Dynamic RAM
Transistor used	Capacitor used
No periodic refreshment	Periodic refreshment
Faster	Slower
Used in cache memory	Used in main memory

b) **A combinational circuit is defined by the functions: F1(A,B,C)=Σ(3,5,6,7) F2= Σ(0,2,4,7) .Implement the circuit with a PLA having 3 inputs, four product terms and 2 outputs.** (7)

(Implementation of the circuit with a PLA- 3 marks)



$F_1 = \Sigma(3,5,6,7)$

$F_2 = \Sigma(0,2,4,7)$

$F_1 = AC + AB + BC$

$F_1' = B'C' + A'C' + A'B'$

$F_2 = \bar{B}\bar{C} + \bar{A}\bar{C} + ABC$

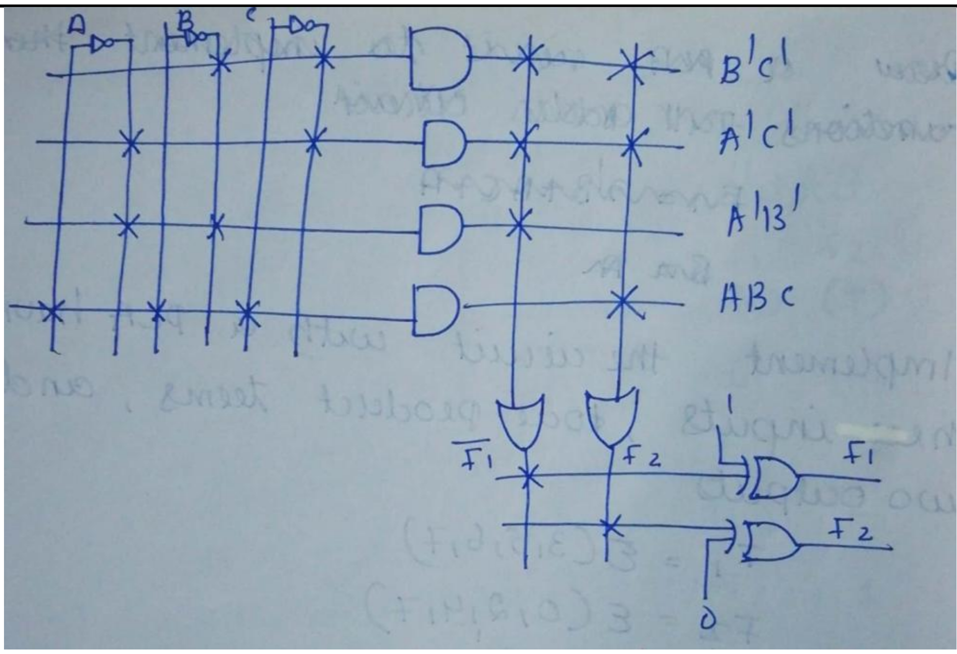
$F_2' = B'C + A'C + ABC$

$\boxed{F_1' F_2 = 4}$

PLA Programming Table.

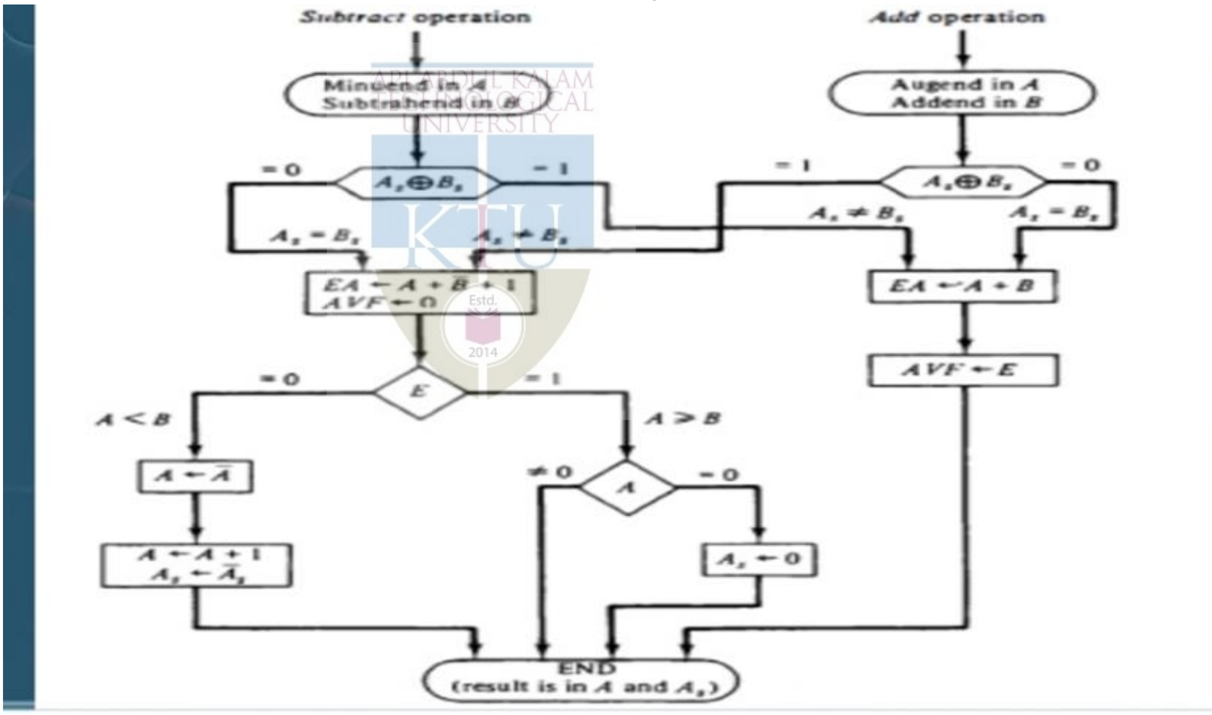
Product term	i/p A B C	output F_1 (C)	F_2 (T)
$B'C'$	– 0 0	1	1
$A'C'$	0 – 0	1	–
$A'B'$	0 0 –	1	1
ABC	1 1 1	–	

Circuit Diagram



20 **With the help of a flowchart explain the addition/subtraction of binary numbers in sign magnitude form.** (10)

(Addition-5 marks Subtraction- 5 marks.(Flow chart/Algorithm)



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