Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

SECOND SEMESTER M.TECH DEGREE EXAMINATION (R,S), MAY 2024

VLSI AND EMBEDDED SYSTEMS

(2021 Scheme)

Course Code: **21VE202**

Course Name: **Advanced CMOS VLSI Design**

Max. Marks: **60** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Define Short Channel Effects. What are the effects of SCE on drain current.
2. Define short circuit power dissipation in MOSFET devices. Write the expression.
3. List any six techniques to reduce leakage reduction.
4. Define race problem in dynamic circuits. How can it be overcome?
5. Show the implementation of XOR/XNOR gates using CPL logic.
6. Sketch the circuit diagram of a 3-input NOR gate in NMOS logic and pseudo-NMOS logic.
7. Identify the major sources of power wastage in SRAM.
8. Compare 6T and 4T SRAM cell.

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

9. Define surface scattering and velocity saturation. Explain how velocity saturation and surface scattering leads to mobility degradation. (6)

OR

10. Explain Drain Induced Barrier Lowering (DIBL) in MOSFET devices. How it leads to punch through. (6)

MODULE II

11. List the components of gate leakage current in MOSFET devices. Explain with suitable diagram. (6)

OR

12. Explain switching power dissipation and glitching power dissipation in MOSFET devices. (6)

MODULE III

13. Analyze a conventional two input CMOS NAND gate circuit and explain stacking effect can be used to reduce leakage power dissipation. (6)

OR

14. With a neat sketch, explain a variable threshold CMOS inverter circuit. (6)

MODULE IV

15. List the disadvantages of domino logic. Implement Y = (A+B) (C+D) (E+F) using the domino logic. (6)

OR

16. Sketch the circuit diagram of NORA CMOS logic and explain how the precharge/evaluation phases scheduled in NORA logic. (6)

MODULE V

17. Apply DCVS technique to implement XOR and XNOR gate. (6)

OR

18. Describe adiabatic logic circuit. Illustrate the energy recovery RC model concept of adiabatic logic circuit (6)

MODULE VI

19. Sketch the schematic diagram of a SRAM memory cell along with sense amplifier. Explain how read operations is performed. (6)

OR

20. Explain with circuit diagram how the read, write and hold operations are performed in SRAM. (6)

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