Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

SECOND SEMESTER M.TECH DEGREE EXAMINATION (R,S), MAY 2024

VLSI AND EMBEDDED SYSTEMS

(2021 Scheme)

Course Code: 21VE204-E

Course Name: Physical Design and Verification

Max. Marks: 60 **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Explain the term synthesis in IC design.
2. Illustrate the significance of static timing analysis in physical design.
3. List the various inputs for routing.
4. Enumerate the different types of floor planning.
5. Explain the significance of clock tree optimization in physical design.
6. Illustrate clock tree synthesis flow.
7. Describe clock tree power consumption.
8. Explain logical equivalence checking associated with physical verification.

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

9. Compare frontend and backend design of an IC. (6)

OR

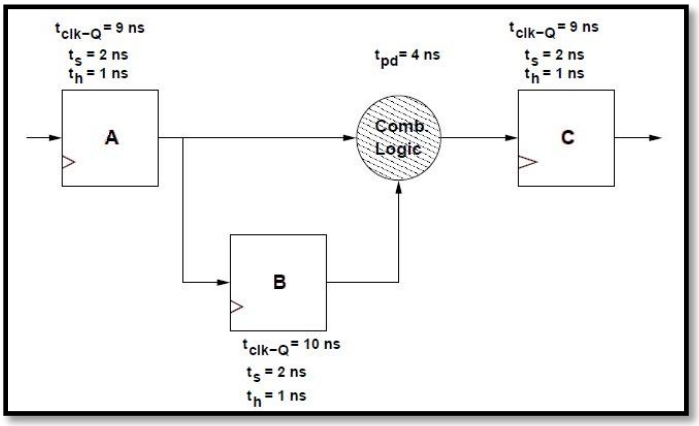
10. Explain command flow of synthesis with an example. (6)

MODULE II

11. Explain static timing analysis and timing violations with relevant diagrams. Illustrate how one can determine the maximum frequency of operation of a circuit. (6)

OR

12. Analyze the following circuit and calculate the maximum clock frequency that can be given to this circuit. (6)



MODULE III

13. Illustrate the following (a) Detailed Routing (b) Post route optimization (6)

OR

14. Demonstrate DRC and LVS in physical design of an IC. (6)

MODULE IV

15. Show the steps of floor planning in physical design with relevant diagrams. (6)

OR

16. Summarize the methods available to control and manage congestion during the placement process. (6)

MODULE V

17. Explain clock tree optimization technique with an example. (6)

OR

18. Illustrate skew balancing with the help of an example. (6)

MODULE VI

19. Illustrate synchronous and cross clock balancing with relevant sketches. (6)

OR

20. Discuss the significance of TCL scripting in physical design with any two example script. (6)

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