Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

SECOND SEMESTER M.TECH DEGREE EXAMINATION (R,S), MAY 2024

VLSI AND EMBEDDED SYSTEMS

(2021 Scheme)

Course Code: 21VE205-C

Course Name: Computer Architecture and Parallel Processing

Max. Marks: 60 **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Outline the layered view of computer design.
2. Illustrate the concept of pipelining and what are the issues in pipelining?
3. Explain VLIW processors.
4. Comment on the various write policies of cache memory.
5. Discuss in brief on the issues regarding cache coherence.
6. Explain about memory hierarchy with a suitable diagram.
7. Explain about the models of memory consistency.
8. Differentiate static and dynamic interconnection networks.

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

9. Explain in brief on Flynn's taxonomy of computer architecture. (6)

OR

10. Explain the various multithreading implementations with suitable diagrams? (6)

MODULE II

11. Design the data path of a single cycle processor for 'sw' instruction and comment on the disadvantages of single cycle processor. (6)

OR

12. Define Amdahl's law? Consider an application where floating point (FP) instructions are responsible for 70% of execution time and FPSQR instructions take 20% of execution time. Compare the two designs given below. (6)
    Design I: FP instructions faster by 2X

Design 2: FPSQR instructions faster by 15X

MODULE III

13. Explain control hazards and discuss the different mitigation techniques used. (6)

OR

14. Explain on superscalar processor organization with neat diagram? (6)

MODULE IV

15. Explain the different methods by which cache performance can be improved. (6)

OR

16. With a neat diagram, explain the address translation using TLB in virtual memory? (6)

MODULE V

17. Give a brief idea on cache coherence issues and discuss on the Directory-based protocol for enforcing cache coherence. (6)

OR

18. Explain in brief on the different distributed memory architectures. (6)

MODULE VI

19. Describe in detail on the various interconnection networks for parallel systems. (6)

OR

20. Explain the concept of Symmetric multithreading with a suitable diagram. (6)

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