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| **Scheme of Valuation/Answer Key** | | | | | |
| **APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**  FOURTH SEMESTER B.TECH DEGREE EXAMINATION, MAY 2019 | | | | | |
| **Course Code: EE204** | | | | | |
| **Course Name: DIGITAL ELECTRONICS AND LOGIC DESIGN (EE)** | | | | | |
| Max. Marks: 100 | | |  | Duration: 3 Hours | |
| **PART A** | | | | | |
|  |  | ***Answer all questions, each carries 5 marks*** | | | Marks |
| 1 |  | Conversion to binary form - 2.5 Marks  Conversion to decimal - 2.5 Marks | | | 5 |
| 2 |  | Truth table - 1 Mark  POS form - F   * 1 Mark   SOP - F =   * 1 Mark   Kmap reduction – writing the K map and reduction in any one form (either SOP or POS) - 2 Marks | | | 5 |
| 3 |  | Race around condition with figure- 3 Marks  Ways to avoid race around condition - 2 Marks | | | 5 |
| 4 |  | Full adder logic table & equation - 3 Marks  3 x 8 decoder table and logic and implementation -2 Marks | | | 5 |
| 5 |  | Johnson or Ring counter (anyone) - logic table and logic diagram (2 + 2 marks)  Explanation - 1 Mark | | | 5 |
| 6 |  | Mealy circuit with state diagram – 1 Mark  Moore circuit with state diagram – 1 Mark  Explanation and difference – 3 Marks | | | 5 |
| 7 |  | Circuit diagram and explanation of 3-bit R-2R ladder circuit – 3 marks  Expression and derivation – 2 Marks | | | 5 |
| 8 |  | Implementation using K-map with AND-OR logic - 5 Marks | | | 5 |
| **PART B** | | | | | |
| ***Answer any two questions, each carries 10 marks*** | | | | | |
| 9 | a) | Range of numbers possible of signed bit, 1s and 2s complement for word length of 8 bits  - Signed bit : to = -127 to +127  - 1’s Complement :to += -127 to +127  - 2’s complement: to = -128 to +127  - 5 Marks (full marks for Ist part)  Second part of the question is incomplete – 2 marks may be given if only 2nd part is attempted. | | | 5 |
|  | b) | Error detection using parity with reference to even parity for ASCII code - 3 Marks  Explain with respect to letter A - 2 Marks | | | 5 |
| 10 | a) | TTL NAND gate figure and explanation (2+ 3 Marks) | | | 5 |
|  | b) | Typing mistake in question – 1 and 5 represented in both minterm and don’t care. Full marks may be given if attempted. | | | 5 |
| 11 | a) | Gray code is not given. Attempt may be given 3 marks. | | | 3 |
|  | b) | K-map after SOP expression – 2 Marks.  K-map reduction – F= - 4 Marks  Logic circuit using NAND gate - 1 Mark | | | 7 |
| **PART C** | | | | | |
| ***Answer any two questions, each carries 10 marks*** | | | | | |
| 12 | a) | Truth table – 1 Mark  K-map - 2 Mark  Implementation using MUX - 2 Marks | | | 5 |
|  | b) | Truth table of full adder - 1 Mark  Full adder using two half adders - 4 Marks | | | 5 |
| 13 | a) | Question is too big to be answered for 5 marks.  Listing the different shift registers – 1 Mark (SISO, SIPO, PISO, PIPO)  Figures and explanation of **any two** shift registers – 4 Marks | | |  |
|  | b) | 3 bit asynchronous counter design up to count 7 – Truth table – 1 Mark  Logic diagram with JK flip flops – 4 Marks | | | 5 |
| 14 | a) | Explanation of glitch with Mod 6 counter – 2 Marks  Mod 6 counter design **with or without** glitch - 3 | | | 5 |
|  | b) | 2:4 Decoder logic table and logic diagram - 2 Marks  1:4 Demux logic table and logic diagram - 2 Marks  Conversion explanation - 1 Mark | | | 5 |
| **PART D** | | | | | |
| ***Answer any two questions, each carries 10 marks*** | | | | | |
| 15 | a) | 4-bit ring counter logic diagram - 3 Marks  Table - 1 mark  Explanation - 1 Mark | | | 5 |
|  | b) | Flash type ADC – explanation with figure (2+3) | | | 5 |
| 16 |  | State table form state diagram - 4 Marks   |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | Q2 | Q1 | Q0 | x | Q2+ | Q1+ | Q0+ | T2 | T1 | T0 | | 0 | 0 | 0 | 0  1 | x  x | x  x | x  x | x  x | x  x | x  x | | 0 | 0 | 1 | 0  1 | x  x | x  x | x  x | x  x | x  x | x  x | | 0 | 1 | 0 | 0  1 | x  x | x  x | x  x | x  x | x  x | x  x | | 0 | 1 | 1 | 0  1 | 1  1 | 1  0 | 0  1 | 1  1 | 0  1 | 1  0 | | 1 | 0 | 0 | 0  1 | x  x | x  x | x  x | x  x | x  x | x  x | | 1 | 0 | 1 | 0  1 | 1  1 | 1  0 | 1  1 | 0  0 | 1  0 | 0  0 | | 1 | 1 | 0 | 0  1 | 1  0 | 0  1 | 1  1 | 0  1 | 1  0 | 1  1 | | 1 | 1 | 1 | 0  1 | 1  0 | 1  1 | 0  1 | 0  1 | 0  0 | 1  0 |   Design for T flip flop using K-map – 4  Logic Diagram - 2 Marks | | | 10 |
| 17 | a) | PLA and PAL (any two points - 2 Marks each) | | | 4 |
|  | b) | VHDL program for full adder – **ANY** approach (6 marks) | | | 6 |
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