Reg No.:		D.: Name:	
		APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY FOURTH SEMESTER B.TECH DEGREE EXAMINATION, JULY 2017	
		Course Code: EC206	
		Course Name: COMPUTER ORGANISATION (EC)	
Max. Marks: 100		Marks: 100 Duration: 3 I PART A	Hours
		Question No.1 is compulsory. Answer question 2 or 3. Each carries 15 marks.	
1	a)	Design a multiplier to multiply two 4-bit numbers. Illustrate with an example.	(8)
	b)	Convert the following MIPS assembly code into machine language. Write the instructions in hexadecimal. addi \$s0, \$0, 73 sw \$t1, -7(\$t2) sub \$t1, \$s7, \$s2	(7)
2	a)	Design a shifter that always shifts a 32 bit input left by 2 bits. The input and output	(6)
		are both 32 bits. Explain the design and sketch a schematic.	
	b)	Show the schematic of a sign extension unit with a 4-bit input and an 8-bit output.	(4)
	c)	Express the following base 10 numbers in IEEE 754 single precision floating-point	(5)
		format:	
		(i) -13.5625 (ii) 42.3125	
		OR	
3	a)	Differentiate Big-Endian and Little-Endian machines.	(3)
	b)	Explain the various instruction formats of MIPS with examples.	(7)
	c)	Give a brief account of the architecture of MIPS.	(5)
		PART B Question No.4 is compulsory. Answer question 5 or 6. Each carries 15 marks.	
4	a)	Explain any three state elements of a MIPS processor.	(5)
	b)	What is an exception? How exceptions are classified and handled?	(7)
	c)	Mention any three advantages of multi cycle implementation compared to single cycle implementation.	(3)
5	a)	Explain various addressing modes of MIPS with examples.	(10)
	b)	What is the range of instruction addresses to which conditional branches such as beq	(5)
		and bne can branch in MIPS? Give your answer in number of instructions relative	
		to the conditional branch instructions.	
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OR

- 6 a) Draw the data path for single cycle processor for R-type instruction along with the (9) control signals. Explain the design procedure for the control unit.
 - b) Draw the datapath for multicycle processor for R-type instruction and explain (6)

PART C

Question No.7 is compulsory. Answer question 8 or 9. Each carries 20 marks.

7 Briefly explain the standard I/O interfaces:-(10)a) (i) Serial port (ii) Parallel port (iii) USB. Explain clearly the address translation mechanism in virtual memory. (10)b) Draw the internal organization of a SRAM cell and explain the read and write (10)8 a) operation. Explain DMA data transfer method. What are the advantages of DMA transfer? b) (10)OR (8) 9 Explain direct mapped cache structure. a) Here is a series of address references given as word addresses: (12)b) 1,4,8,5,20,17,19,56,9,11,4,43,5,6,9,17. Assuming a direct mapped cache with 16 one-word blocks that is initially empty,

Assuming a direct mapped cache with 16 one-word blocks that is initially empty, label each reference in the list as a hit or a miss and show the final contents of the cache.
